

NTR5103N

MOSFET – Single, N-Channel, Small Signal, SOT-23

60 V, 310 mA

Features

- Low $R_{DS(on)}$
- Small Footprint Surface Mount Package
- Trench Technology
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Low Side Load Switch
- Level Shift Circuits
- DC-DC Converter
- Portable Applications i.e. DSC, PDA, Cell Phone, etc.

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

| Rating | Symbol | Value | Unit |
|--|----------------|--------------------------|------------------|
| Drain-to-Source Voltage | V_{DSS} | 60 | V |
| Gate-to-Source Voltage | V_{GS} | ± 30 | V |
| Drain Current (Note 1) Steady State | I_D | $T_A = 25^\circ\text{C}$ | 260 |
| | | $T_A = 85^\circ\text{C}$ | 190 |
| $t < 5$ s | I_D | $T_A = 25^\circ\text{C}$ | 310 |
| | | $T_A = 85^\circ\text{C}$ | 220 |
| Power Dissipation (Note 1) Steady State | P_D | $t < 5$ s | 300 |
| | | | 420 |
| Pulsed Drain Current ($t_p = 10 \mu\text{s}$) | I_{DM} | 1.2 | A |
| Operating Junction and Storage Temperature Range | T_J, T_{STG} | -55 to +150 | $^\circ\text{C}$ |
| Source Current (Body Diode) | I_S | 300 | mA |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | T_L | 260 | $^\circ\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|--|-----------------|-----|---------------------------|
| Junction-to-Ambient – Steady State (Note 1) | $R_{\theta JA}$ | 417 | $^\circ\text{C}/\text{W}$ |
| Junction-to-Ambient – $t \leq 5$ s (Note 1) | $R_{\theta JA}$ | 300 | |

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)

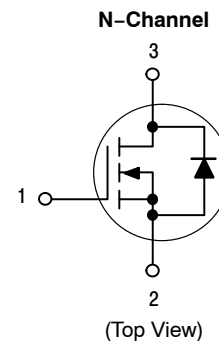


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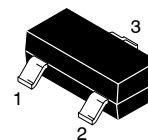
<http://onsemi.com>

| $V_{(BR)DSS}$ | $R_{DS(on)}$ MAX | I_D MAX (Note 1) |
|---------------|----------------------|-----------------------|
| 60 V | 3.0 Ω @ 4.5 V | 310 mA |
| | 2.5 Ω @ 10 V | |

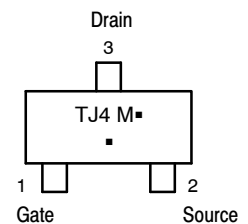
Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



SOT-23
CASE 318
STYLE 21



TJ4 = Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

| Device | Package | Shipping† |
|-------------|---------------------|--------------------|
| NTR5103NT1G | SOT-23 (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTR5103N

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|-------------------|--|---------------------------|-----|-----|----------------------------|
| OFF CHARACTERISTICS | | | | | | |
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ | 60 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | | | 75 | | $\text{mV}/^\circ\text{C}$ |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{GS} = 0\text{ V},$ $V_{DS} = 60\text{ V}$ | $T_J = 25^\circ\text{C}$ | | 1 | μA |
| | | | $T_J = 125^\circ\text{C}$ | | 500 | |
| Gate-to-Source Leakage Current | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = \pm 30\text{ V}$ | | | 200 | nA |

ON CHARACTERISTICS (Note 2)

| | | | | | | |
|--|------------------|---|-----|-----|-----|----------------------------|
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$ | 1.9 | | 2.6 | V |
| Negative Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | | | 4.4 | | $\text{mV}/^\circ\text{C}$ |
| Drain-to-Source On Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 240\text{ mA}$ | | 1.0 | 2.5 | Ω |
| | | $V_{GS} = 4.5\text{ V}, I_D = 50\text{ mA}$ | | 1.4 | 3.0 | |
| Forward Transconductance | g_{FS} | $V_{DS} = 5\text{ V}, I_D = 200\text{ mA}$ | | 530 | | mS |

CHARGES AND CAPACITANCES

| | | | | | | |
|------------------------------|--------------|---|--|------|----|-------------|
| Input Capacitance | C_{ISS} | $V_{GS} = 0\text{ V}, f = 1\text{ MHz},$ $V_{DS} = 25\text{ V}$ | | 26.7 | 40 | pF |
| Output Capacitance | C_{OSS} | | | 4.6 | | |
| Reverse Transfer Capacitance | C_{RSS} | | | 2.9 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS} = 5\text{ V}, V_{DS} = 10\text{ V};$ $I_D = 240\text{ mA}$ | | 0.81 | | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | 0.31 | | |
| Gate-to-Source Charge | Q_{GS} | | | 0.48 | | |
| Gate-to-Drain Charge | Q_{GD} | | | 0.08 | | |

SWITCHING CHARACTERISTICS, $V_{GS} = V$ (Note 3)

| | | | | | | |
|---------------------|--------------|--|--|-----|--|----|
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{GS} = 10\text{ V}, V_{DD} = 30\text{ V},$ $I_D = 200\text{ mA}, R_G = 10\ \Omega$ | | 1.7 | | ns |
| Rise Time | t_r | | | 1.2 | | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | 4.8 | | |
| Fall Time | t_f | | | 3.6 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|-----------------------|----------|---|--------------------------|--|------|-----|---|
| Forward Diode Voltage | V_{SD} | $V_{GS} = 0\text{ V},$ $I_S = 200\text{ mA}$ | $T_J = 25^\circ\text{C}$ | | 0.79 | 1.2 | V |
| | | | $T_J = 85^\circ\text{C}$ | | 0.7 | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

3. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

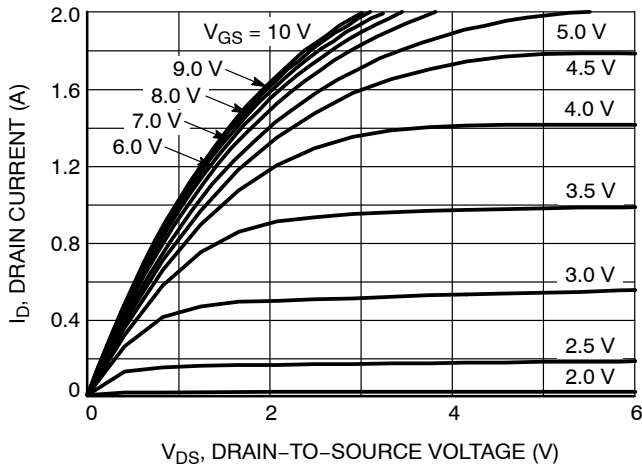


Figure 1. On-Region Characteristics

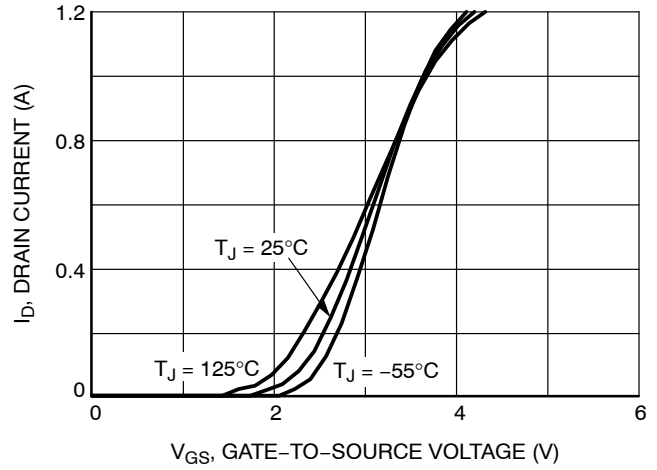


Figure 2. Transfer Characteristics

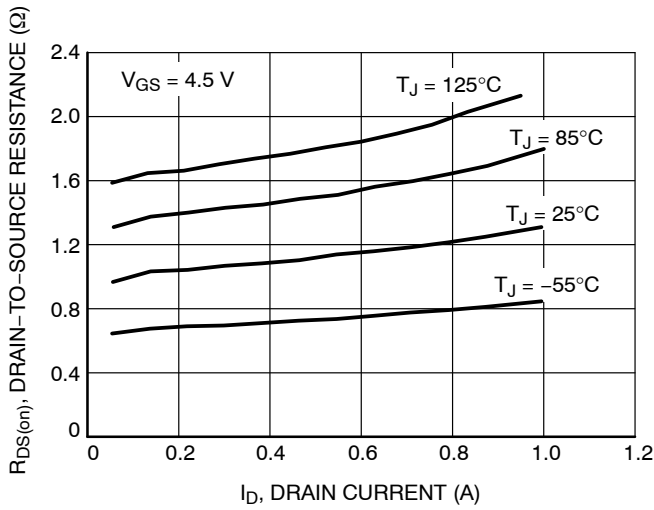


Figure 3. On-Resistance vs. Drain Current and Temperature

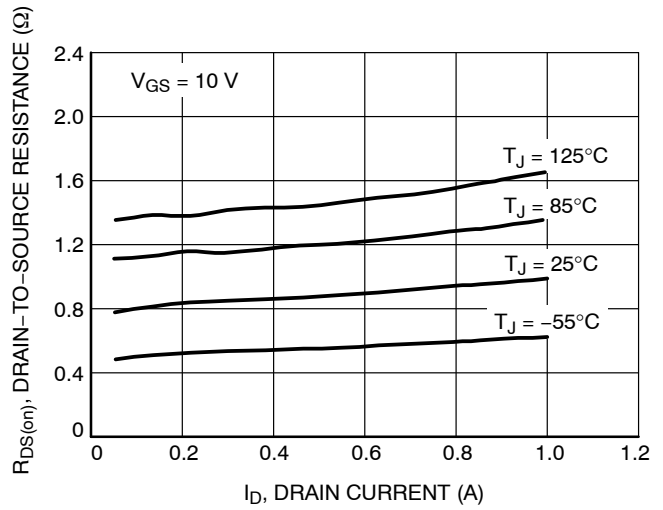


Figure 4. On-Resistance vs. Drain Current and Temperature

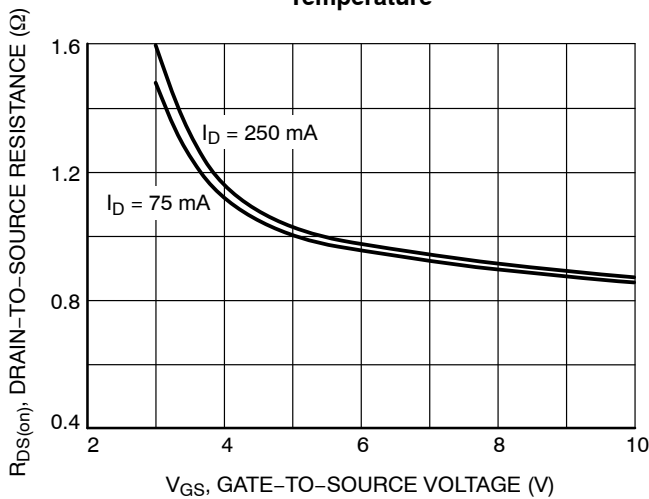


Figure 5. On-Resistance vs. Gate-to-Source Voltage

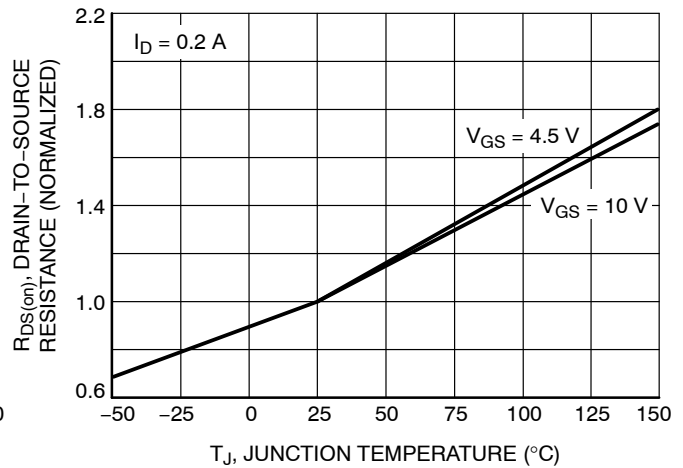


Figure 6. On-Resistance Variation with Temperature

NTR5103N

TYPICAL CHARACTERISTICS

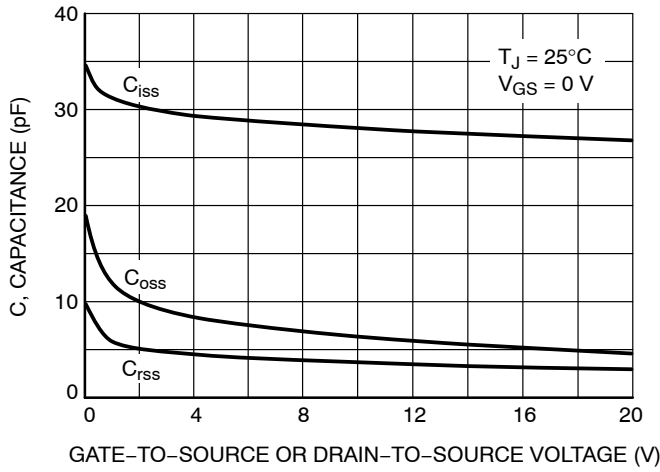


Figure 7. Capacitance Variation

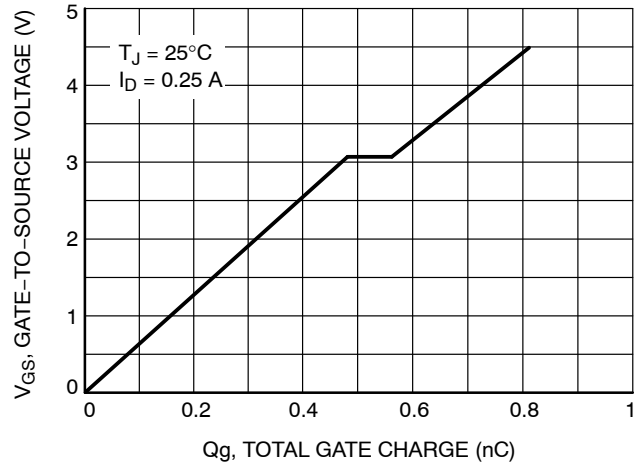


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

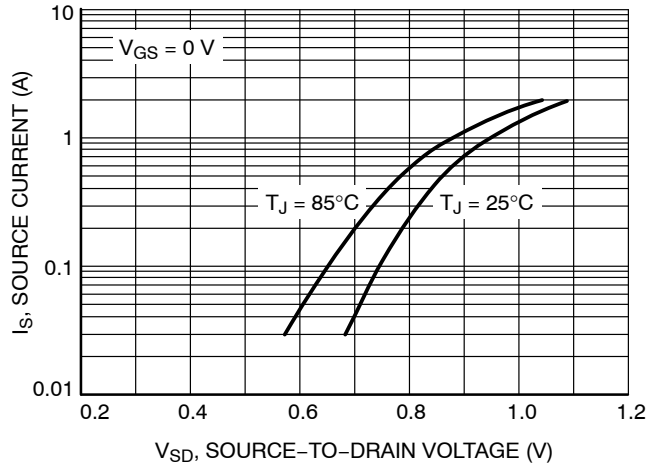


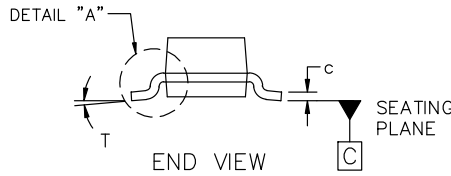
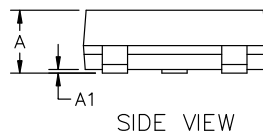
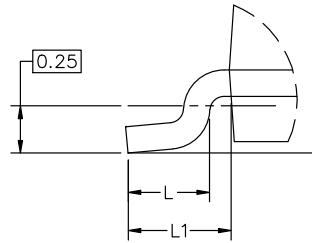
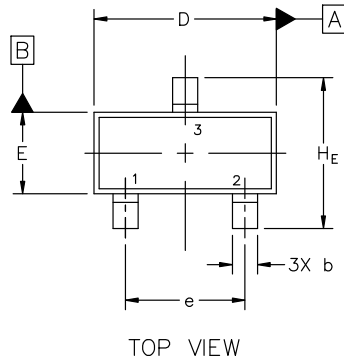
Figure 9. Diode Forward Voltage vs. Current



SCALE 4:1

SOT-23 (TO-236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

DATE 14 AUG 2024

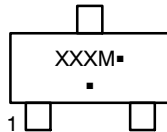


| MILLIMETERS | | | |
|-------------|------|------|------|
| DIM | MIN | NOM | MAX |
| A | 0.89 | 1.00 | 1.11 |
| A1 | 0.01 | 0.06 | 0.10 |
| b | 0.37 | 0.44 | 0.50 |
| c | 0.08 | 0.14 | 0.20 |
| D | 2.80 | 2.90 | 3.04 |
| E | 1.20 | 1.30 | 1.40 |
| e | 1.78 | 1.90 | 2.04 |
| L | 0.30 | 0.43 | 0.55 |
| L1 | 0.35 | 0.54 | 0.69 |
| HE | 2.10 | 2.40 | 2.64 |
| T | 0° | --- | 10° |

NOTES:

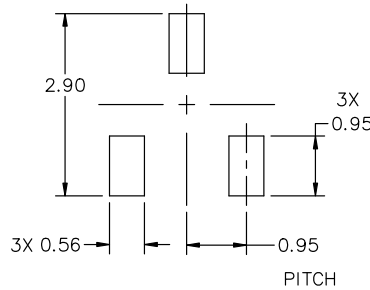
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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- | | | | | | |
|---|---|---|---|---|---|
| STYLE 1 THRU 5: CANCELLED | STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR | STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR | STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE | | |
| STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE | STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE | STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE | STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE | STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE | STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE |
| STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE | STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE | STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE | STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE | STYLE 19: PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE | STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE |
| STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN | STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT | STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE | STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE | STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE | STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION |
| STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE | STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE | | | | |

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