TGA2576-2-FL

2.5 – 6.0 GHz 40 W GaN Power Amplifier

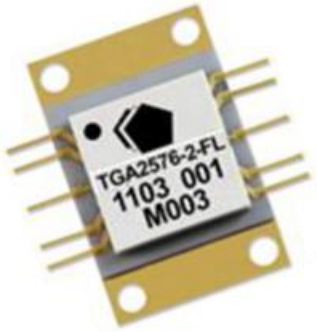
Product Overview

Qorvo's TGA2576-2-FL is a wideband power amplifier fabricated on Qorvo's proven 0.25um GaN on SiC production technology. Operating from 2.5 to 6 GHz, the TGA2576-2-FL achieves 40W of saturated output power, greater than 36% power-added efficiency and 29dB small signal gain.

For ideal thermal management and handling, the TGA2576-2-FL is offered in a CuW-based flanged packaged and can operate in both CW and pulsed modes.

Both RF ports are fully matched to 50Ω, the TGA2576-2-FL is ideally suited to support a variety of commercial and defense related applications.

Lead-free and RoHS compliant.

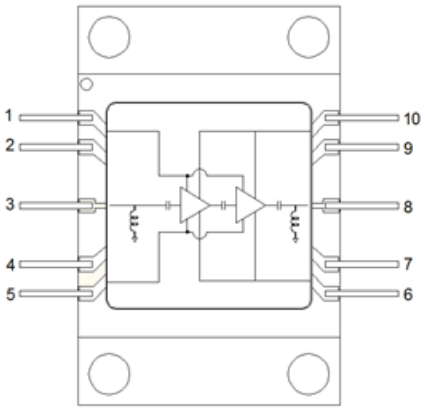


Key Features

- Frequency Range: 2.5 to 6 GHz
- P_{SAT}: 46.5 dBm (P_{IN} = 26 dBm)
- PAE: 36% (P_{IN} = 26 dBm)
- Small Signal Gain: 29 dB
- Bias: Pulse V_D = 30 V, I_{DQ} = 1.55 A
- Dimensions: 11.4 x 17.3 x 3.0 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Communications
- Electronic Warfare
- Test Instrumentation
- EMC Amplifier

Ordering Information

Part No.	Description
TGA2576-2-FL	2.5–6.0 GHz 40 Watt GaN Power Amplifier
TGA2576-2-FL EVB	Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage (V_D)	40 V
Gate Voltage (V_G)	−8 to 0 V
Drain Current (I_D)	5000 mA
Gate Current (I_G)	See plot, page 6
Power Dissipation (P_{DISS})	93 W
RF Input Power, CW, Output Load 50 Ω, V_D = 30 V, I_{DQ} = 1.55 A, T = 85 °C	32 dBm
RF Input Power, CW, Output Load VSWR = 3:1, V_D = 30 V, I_{DQ} = 1.55 A, T = 85 °C	27 dBm
Soldering Temperature (leads)	260 °C
Storage Temperature	−40 to +150 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min
Drain Voltage (V_D)	30 V
Drain Current (I_{DQ})	1550 mA
Drain Current (I_{D_DRIVE})	4300 mA
Operating Temperature	−40 to +85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

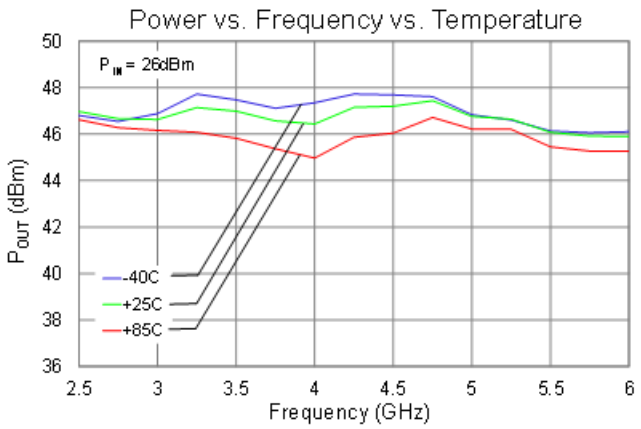
Electrical Specifications

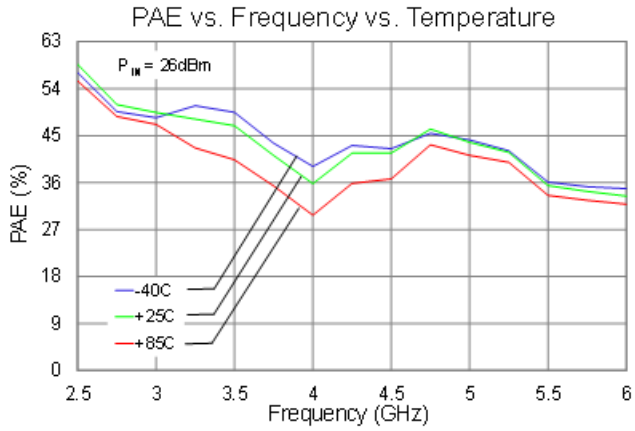
Parameter	Min	Typ	Max	Units
Operational Frequency Range	2.5		6.0	GHz
Small Signal Gain		29		dB
Output Power @ Saturation (Pin = 26 dBm)		46.5		dBm
Power-Added Efficiency (midband; Pin = 26 dBm)		36		%
Gate Leakage (V_D = 10 V, V_G = −3.7 V)	−20		−0.0001	mA
Small Signal Gain Temperature Coefficient		−0.02		dB/°C
Output Power Temperature Coefficient		−0.02		dBm/°C

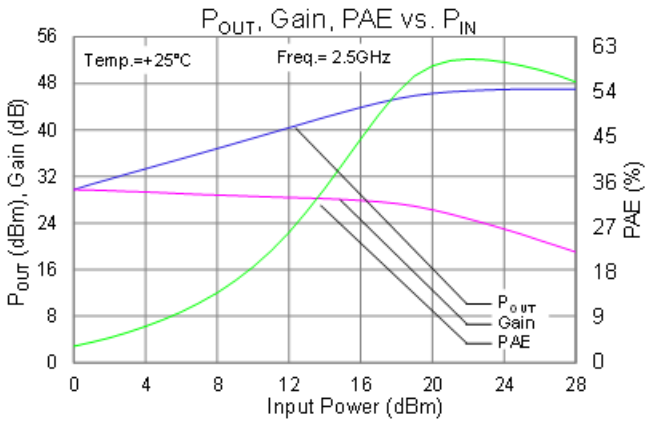
Notes:
Test conditions unless otherwise noted: T=25 °C, V_D = 30 V, I_{DQ} = 1550 mA, CW operation

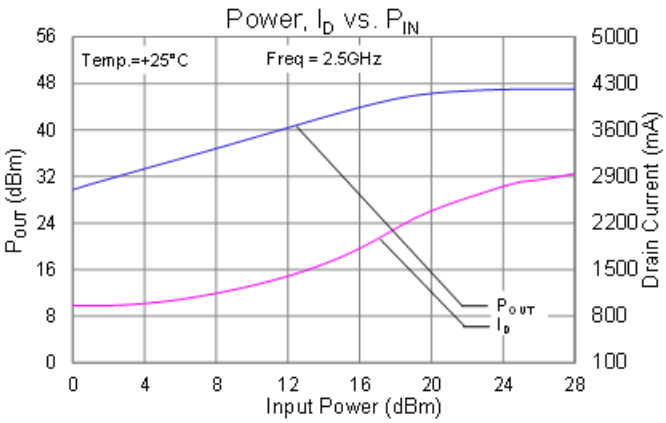
Performance Plots – Large Signal

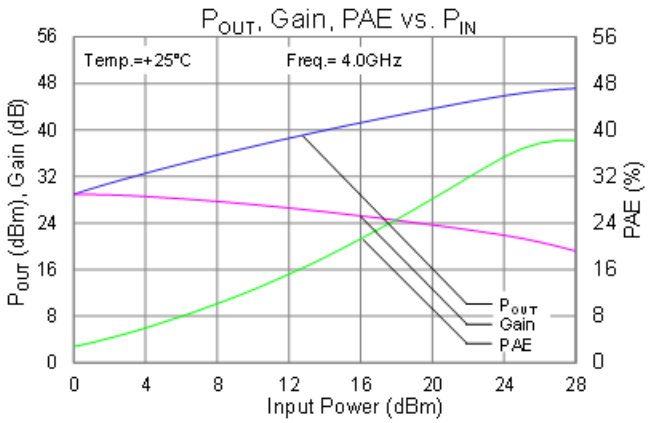
Test conditions unless otherwise noted: T=25 °C, V_D = 30 V, I_{DQ} = 1550 mA, CW

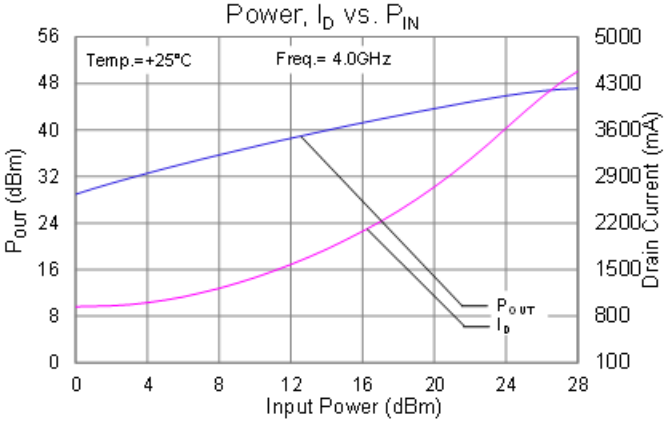






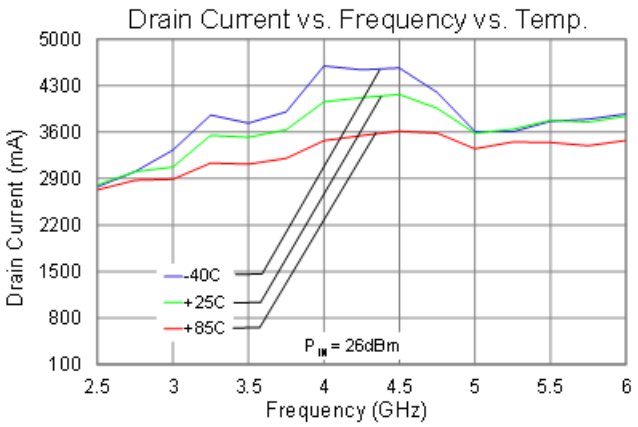


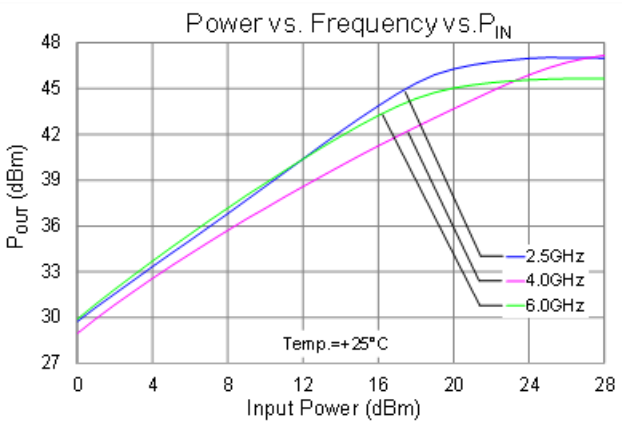




Performance Plots – Large Signal

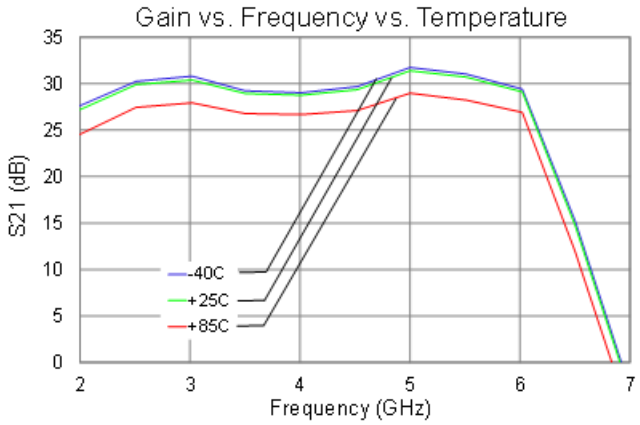
Test conditions unless otherwise noted: T=25 °C, V_D = 30 V, I_{DQ} = 1550 mA, CW

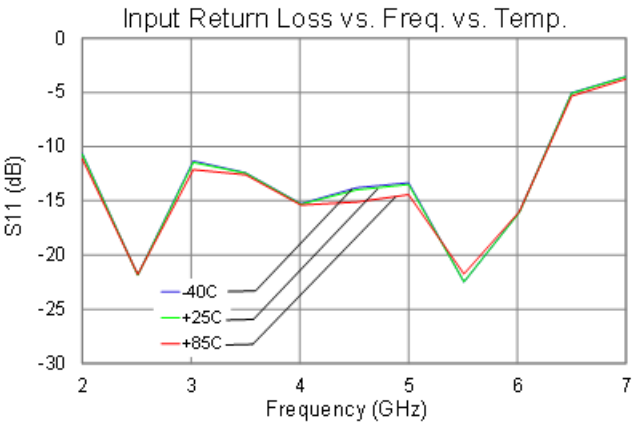


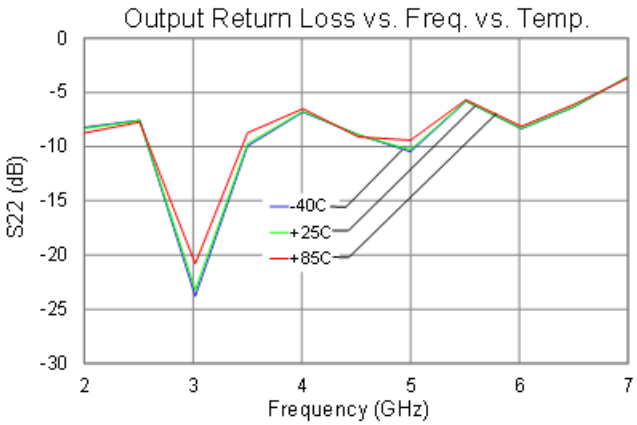


Performance Plots – Small Signal

Test conditions unless otherwise noted: T=25 °C, V_D = 30 V, I_{DQ} = 1550 mA





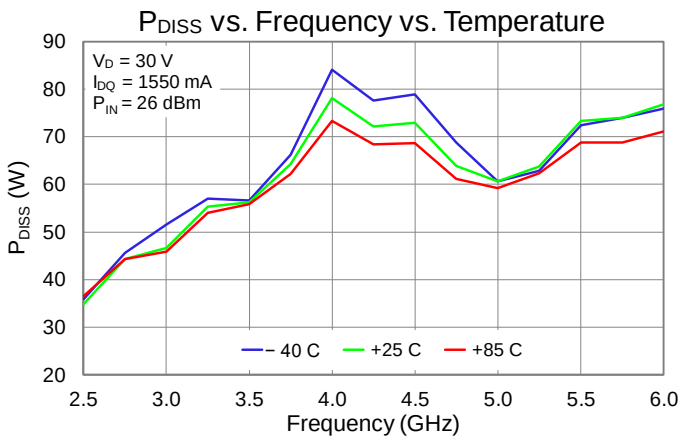


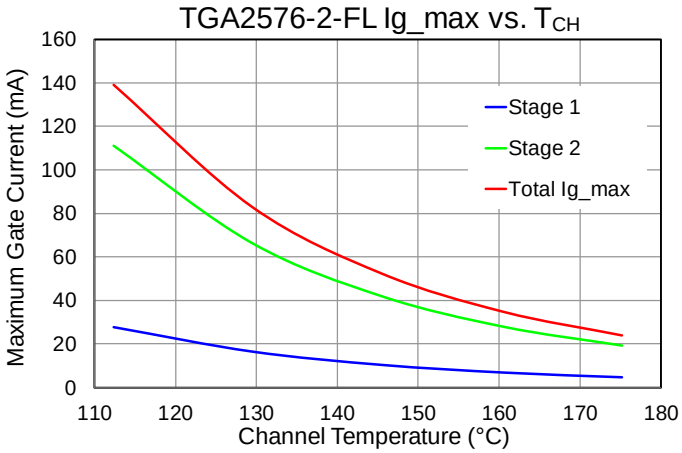
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_D = 30 V, I_{DQ} = 1550 mA, I_{D_Drive} = 3600 mA, P_{OUT} = 46 dBm, P_{DISS} = 72 W	1.245	ºC/W
Channel Temperature, T_{CH} (Under RF Drive) (2)		174.6	°C

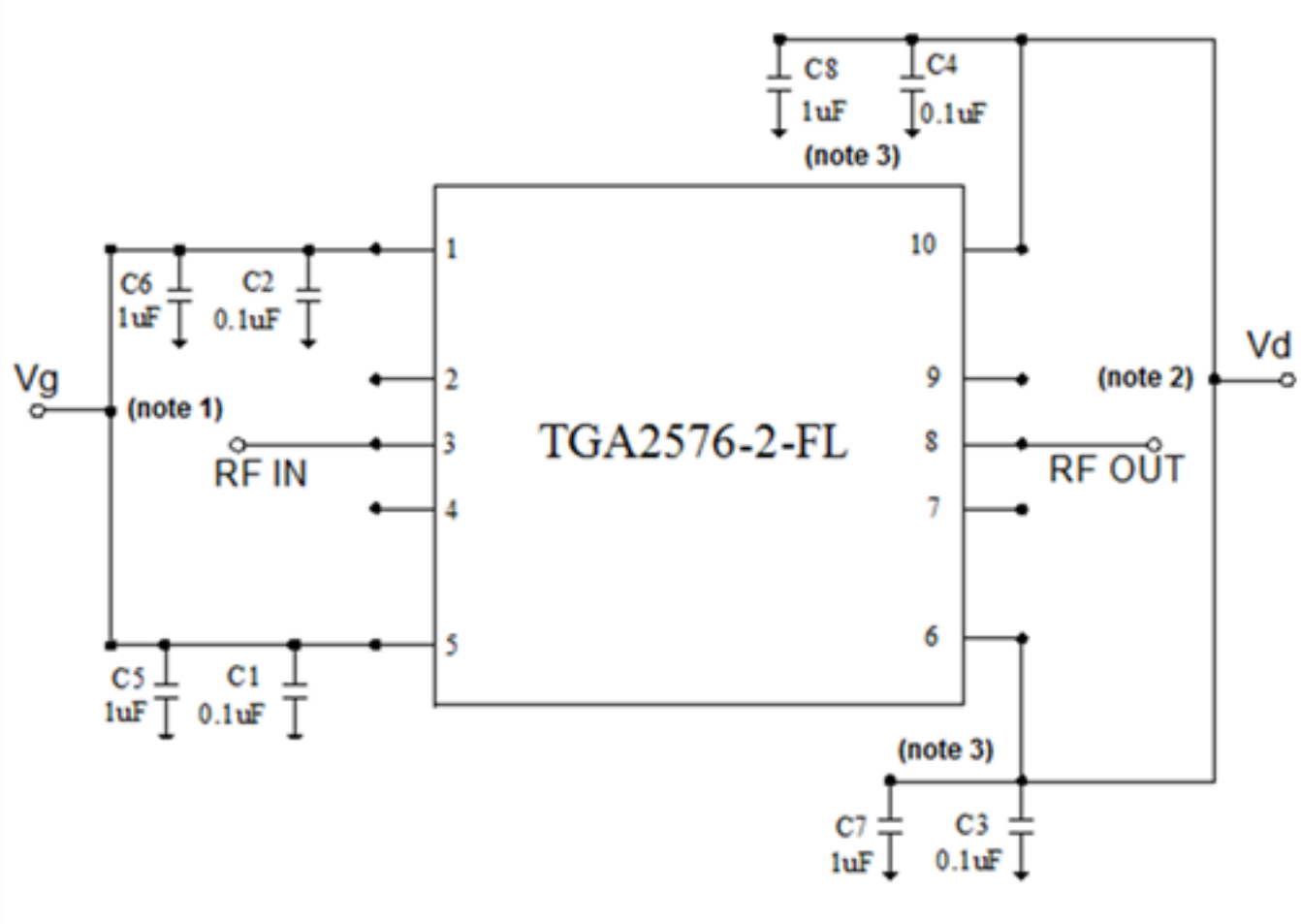
Notes:
1. Thermal resistance referenced to the back of the package (T = 85 °C).
2. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Dissipated Power and Maximum Gate Current





Applications Information



Notes:

1. V_G can be biased from both sides (Pins 1 and 5)
2. V_D must be biased from both sides (Pins 6 and 10)
3. C7 and C8 may be removed for pulsed drain operation.

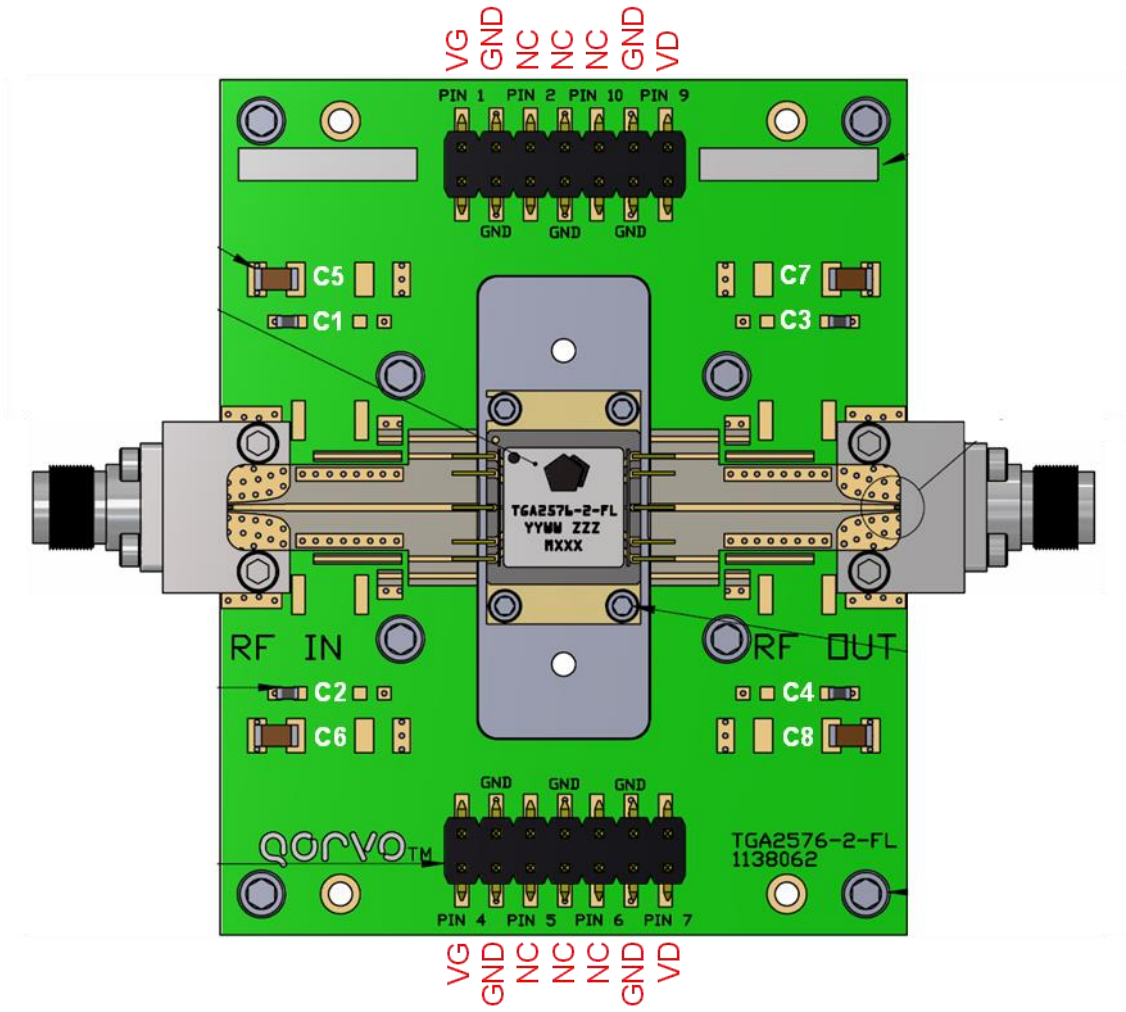
Bias-Up Procedure

1. Set power supply: I_D limit to 5 A, I_G limit to 10 mA
2. Apply −5.0 V to V_G (for pinch-off)
3. Increase V_D to +30 V; Ensure I_{DQ} < 10 mA
4. Adjust V_G more positive until I_{DQ} = 1550 mA
5. Apply RF signal

Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to −5.0 V; Ensure I_{DQ} ~ 0 mA
3. Reduce V_D to 0 V
4. Turn off V_G supply

Evaluation Board (EVB) Layout Assembly

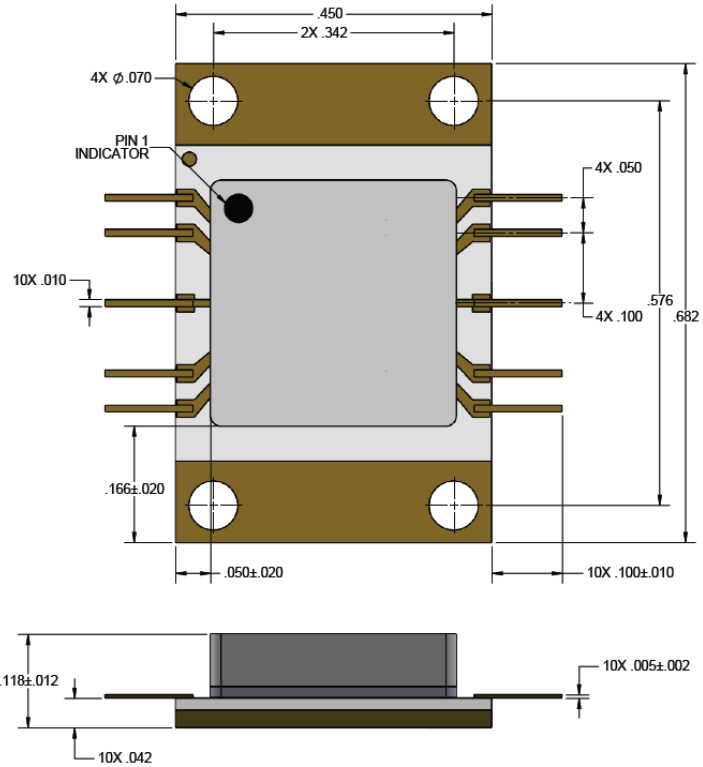


Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1 - C4	0.1 µF	Cap, 0603, 50 V, 10%, X7R	Various	
C5 – C8	1 µF	Cap, 1206, 50 V, 10%, X7R	Various	
J1, J2	2.92 mm	Female End Launch Connector	Southwest Microwave	1092-01A-5

Note: Can remove C7, C8 for pulsed operation

Mechanical Information and Bond Pad Description



Marking:

Part number:	TGA2576-2-FL
Year/Week/Serial number:	YYWW ZZZ
Batch ID:	MXXX

Notes:

1. Unless specified otherwise, dimensions are in inches
2. Unless specified otherwise, tolerances are ± 0.005
3. Materials:

Package base material:	Copper-Tungsten (Cu-W)	Package leads:	Kovar
Package base finish:	Gold Plating	Package lid:	LCP with epoxy

Package Lead Description

Pad No.	Symbol	Description
1, 5	V_G	Gate voltage (1)
2, 4, 7, 9	NC	No internal connection; may be grounded or left open on PCB
3	RF_{IN}	RF Input; matched to 50 Ω; DC shorted to ground
6, 10	V_D	Drain voltage (2)
8	RF_{OUT}	RF Output; matched to 50 Ω; DC shorted to ground
	Package Base	RF and DC ground

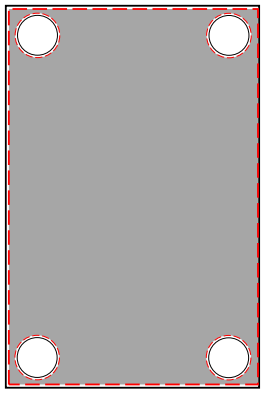
Notes:

1. Bias network is required; must be biased from both sides (Pins 1 and 5); see Application Circuit on page 7
2. Bias network is required; must be biased from both sides (Pins 6 and 10); see Application Circuit on page 7

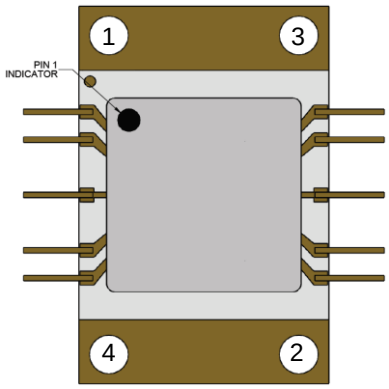
Assembly Notes

1. Carefully clean the PC board, mounting surface, and package leads with 90% (or higher) isopropyl alcohol. Allow it to dry fully.

2. To improve the thermal and RF performance, Qorvo recommends attaching the amplifier to a heat sink, and apply either a thermal compound (Arctic Silver 5 recommended) or a .004 inch (maximum thickness) indium shim between the heat sink and the package. If using an indium shim, the overall dimensions should be no larger than the package base, with clearance holes for the mounting screws. Cut the indium shim material by whatever means are convenient (razor blade, pre-purchased cut pieces, etc.), using the outline of the package base as a guideline (see the figure below; gray area is the indium shim). The shim can be cut a few mils undersize to allow for tolerance in the placement, but the shim must cover the full area of the base, *especially under the 4 mounting screws*. Cutting the shim too small (covering just the center area of the component base or leaving the corners unsupported) may result in deformation of the package base when the mounting screws are tightened, causing poor thermal conductivity due to bowing of the base, and possible attachment issues with the various components inside the package.



3. Use 0-80 screws to attach the component to the next level assembly (heat sink, module, etc.). Use the following tightening pattern:



(There are many variables in a second level assembly that Qorvo does not control, so Qorvo does not recommend an absolute torque value.)

4. The component leads should be manually soldered. Apply a low residue solder alloy meeting J-STD-001 (ROL0, ROL1 or equivalent) with a liquidus temperature below 220 °C to each pin of the TGA2576-2-FL. The use of low residue/no-clean flux (ROL0, ROL1) is recommended. Each solder connection should be completed within 2 to 5 seconds. Adding flux during hand soldering of the component leads with localized spot cleaning is acceptable. Soldering irons meeting the requirements of J-STD-001, Appendix A are acceptable.

5. The packaged part should not be subjected to conventional SMT automated solder reflow processes.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1B	ESDA / JEDEC JS-001-2012
MSL – Moisture Sensitivity Level	NA	

Caution!
ESD-Sensitive Device

Solderability

The component leads should be manually soldered, and the package should not be subjected to conventional reflow processes. Soldering of the component leads is compatible with the latest version of J-STD-020, lead-free solder, 260 °C. The use of no-clean solder to avoid washing after soldering is highly recommended.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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