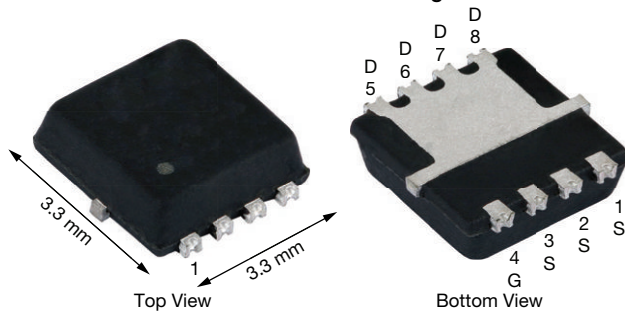
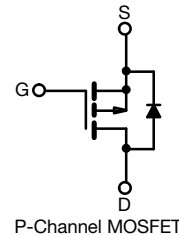


Automotive P-Channel 60 V (D-S) 175 °C MOSFET

PowerPAK® 1212-8W Single

Marking code: Q057
FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE


RoHS COMPLIANT HALOGEN FREE


PRODUCT SUMMARY	
V _{DS} (V)	-60
R _{DS(on)} (Ω) at V _{GS} = -10 V	0.065
R _{DS(on)} (Ω) at V _{GS} = -4.5 V	0.090
I _D (A)	-16
Configuration	Single
Package	PowerPAK 1212-8W

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	-60	V
Gate-source voltage	V _{GS}	± 20	
Continuous drain current	I _D	T _C = 25 °C ^a	-16
		T _C = 125 °C	-11.5
Continuous source current (diode conduction) ^a	I _S	-16	A
Pulsed drain current ^b	I _{DM}	-64	
Single pulse avalanche current	I _{AS}	-23	
Single pulse avalanche energy	E _{AS}	26	mJ
Maximum power dissipation	P _D	T _C = 25 °C	
		T _C = 125 °C	17
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^d		260	

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R _{thJA}	81	°C/W
Junction-to-case (drain)	R _{thJC}	2.8	

Notes

- Package limited
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection



SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = -250\text{ }\mu\text{A}$	-60	-	-	V	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	-1.5	-2.0	-2.5		
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA	
Zero gate voltage drain current	I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = -60\text{ V}$	-	-	-1	μA
		$V_{GS} = 0\text{ V}$	$V_{DS} = -60\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	-50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = -60\text{ V}$, $T_J = 175\text{ }^\circ\text{C}$	-	-	-150	
On-state drain current ^a	$I_{D(on)}$	$V_{GS} = -10\text{ V}$	$V_{DS} \leq -5\text{ V}$	-15	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -5.7\text{ A}$	-	0.049	0.065	Ω
		$V_{GS} = -10\text{ V}$	$I_D = -5.7\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	0.110	
		$V_{GS} = -10\text{ V}$	$I_D = -5.7\text{ A}$, $T_J = 175\text{ }^\circ\text{C}$	-	-	0.136	
		$V_{GS} = -4.5\text{ V}$	$I_D = -4.4\text{ A}$	-	0.069	0.090	
Forward transconductance ^b	g_{fs}	$V_{DS} = -15\text{ V}$, $I_D = -5.7\text{ A}$		-	13	-	S
Dynamic ^b							
Input capacitance	C_{ISS}	$V_{GS} = 0\text{ V}$	$V_{DS} = -25\text{ V}$, $f = 1\text{ MHz}$	-	1083	1385	μF
Output capacitance	C_{OSS}			-	132	165	
Reverse transfer capacitance	C_{RSS}			-	80	105	
Total gate charge ^c	Q_g	$V_{GS} = -10\text{ V}$	$V_{DS} = -30\text{ V}$, $I_D = -5.7\text{ A}$	-	25.5	38	nC
Gate-source charge ^c	Q_{gs}			-	4.3	-	
Gate-drain charge ^c	Q_{gd}			-	6.4	-	
Gate resistance	R_g	f = 1 MHz		3.0	5.6	8.3	Ω
Turn-on delay time ^c	$t_{d(on)}$	$V_{DD} = -30\text{ V}$, $R_L = 30\text{ }\Omega$ $I_D \cong -1\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 1\text{ }\Omega$		-	9	14	ns
Rise time ^c	t_r			-	5	10	
Turn-off delay time ^c	$t_{d(off)}$			-	39	60	
Fall time ^c	t_f			-	8	12	
Source-drain diode ratings and characteristics ^b							
Pulsed current ^a	I_{SM}			-	-	-64	A
Forward voltage	V_{SD}	$I_F = -6\text{ A}$, $V_{GS} = 0\text{ V}$		-	-0.85	-1.2	V
Body diode reverse recovery time	t_{rr}	$I_F = -2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		-	26	52	ns
Body diode reverse recovery charge	Q_{rr}			-	35	70	nC
Reverse recovery fall time	t_a			-	21	-	ns
Reverse recovery rise time	t_b			-	5	-	
Body diode peak reverse recovery current	$I_{RM(REC)}$					-	-3.2

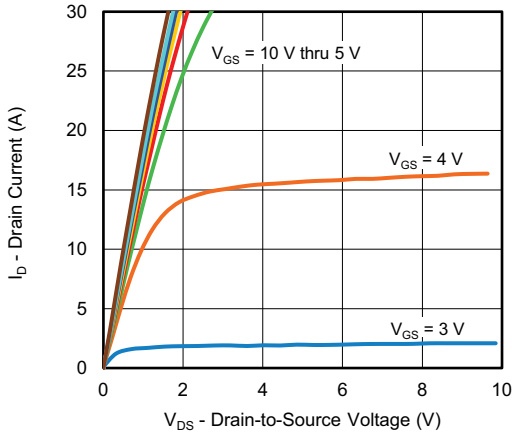
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

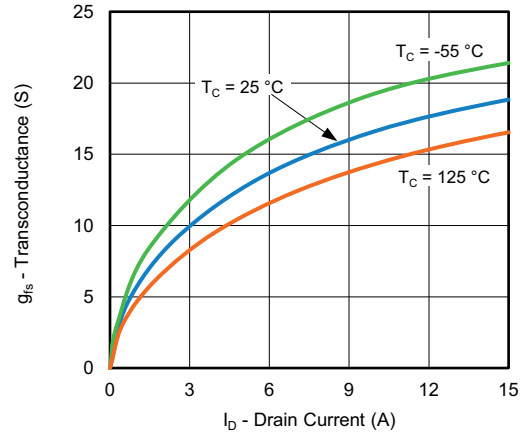
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



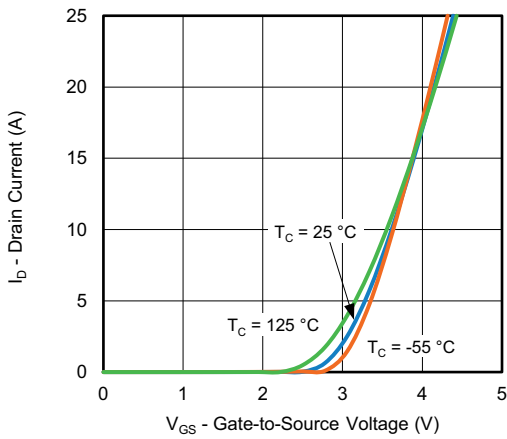
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



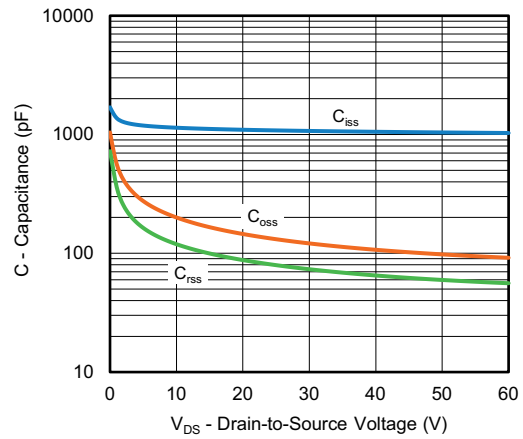
Output Characteristics



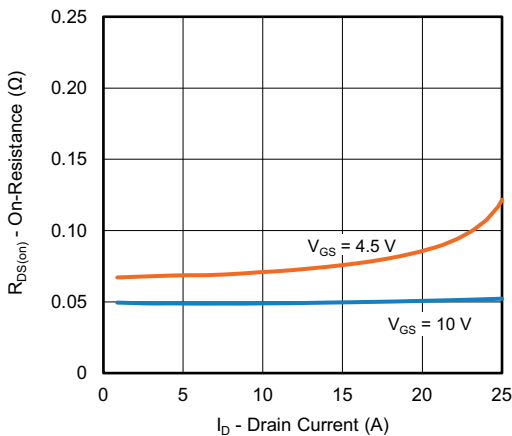
Transconductance



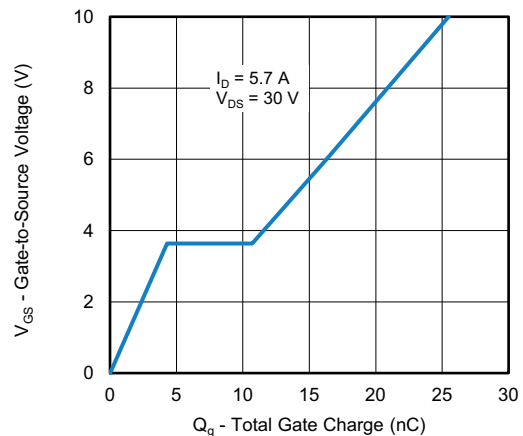
Transfer Characteristics



Capacitance

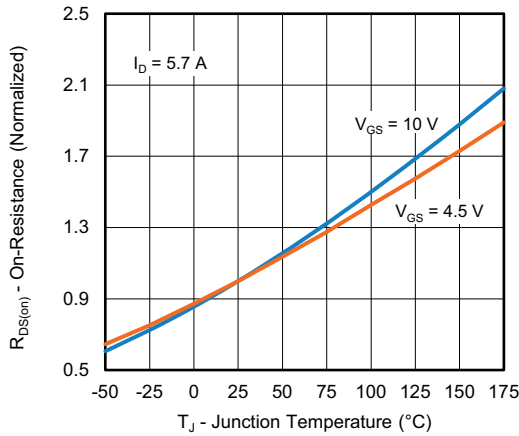


On-Resistance vs. Drain Current

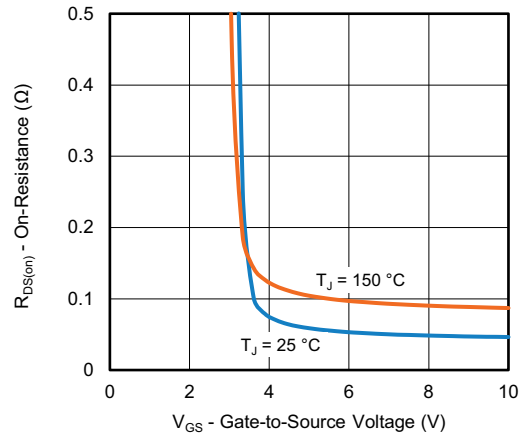


Gate Charge

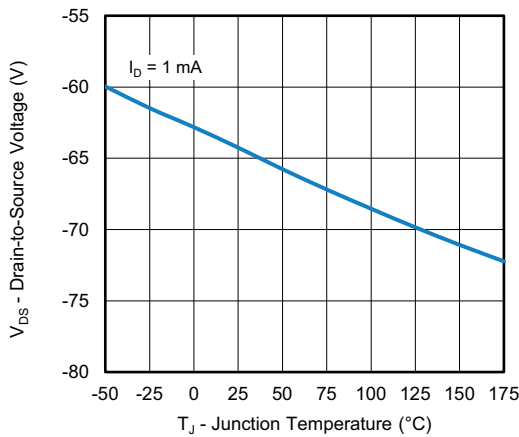
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



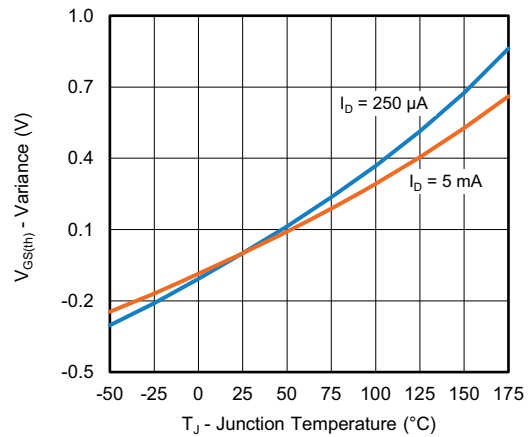
On-Resistance vs. Junction Temperature



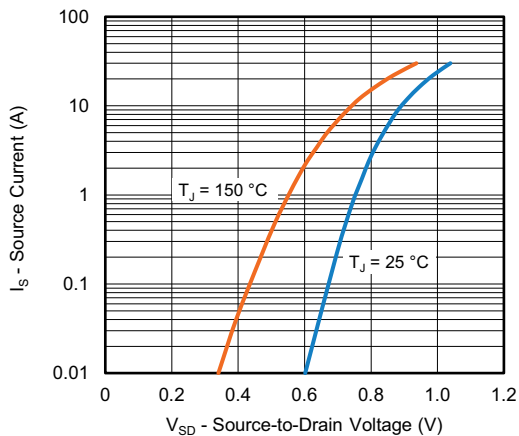
On-Resistance vs. Gate-to-Source Voltage



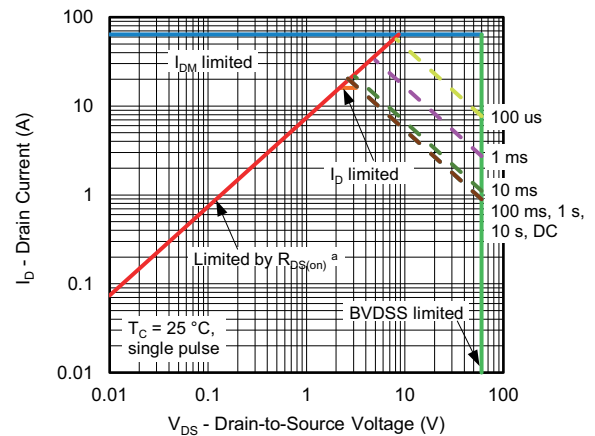
Drain Source Breakdown vs. Junction Temperature



Threshold Voltage



Source Drain Diode Forward Voltage



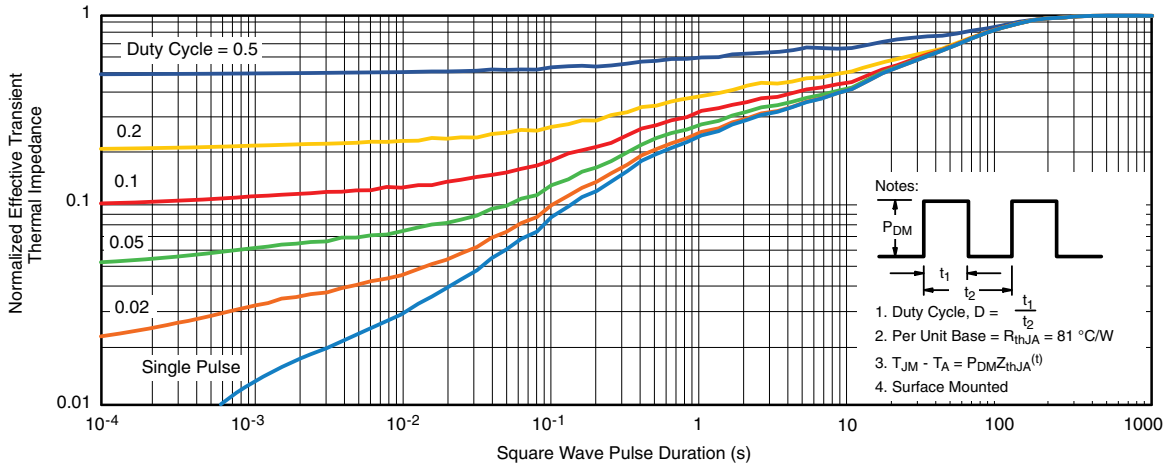
Safe Operating Area

Note

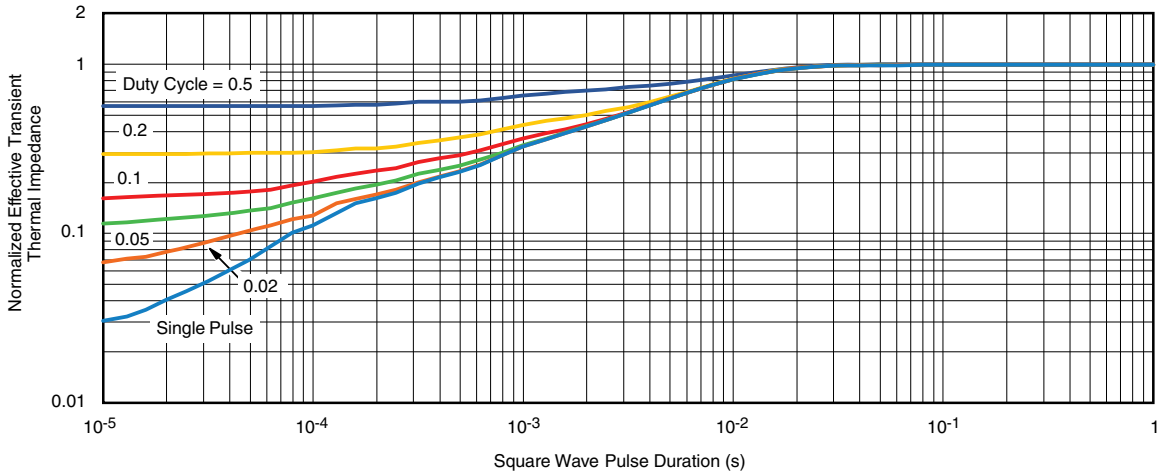
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



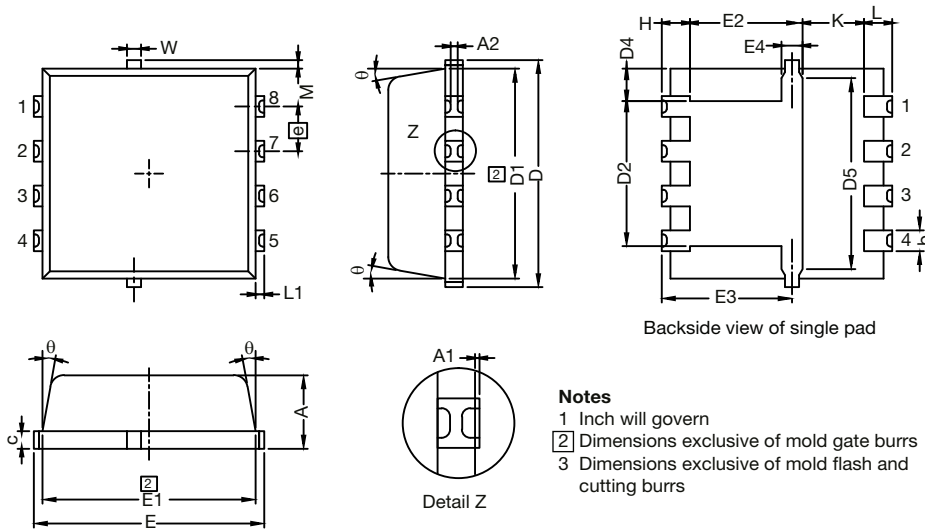
Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^\circ\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^\circ\text{C}$)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

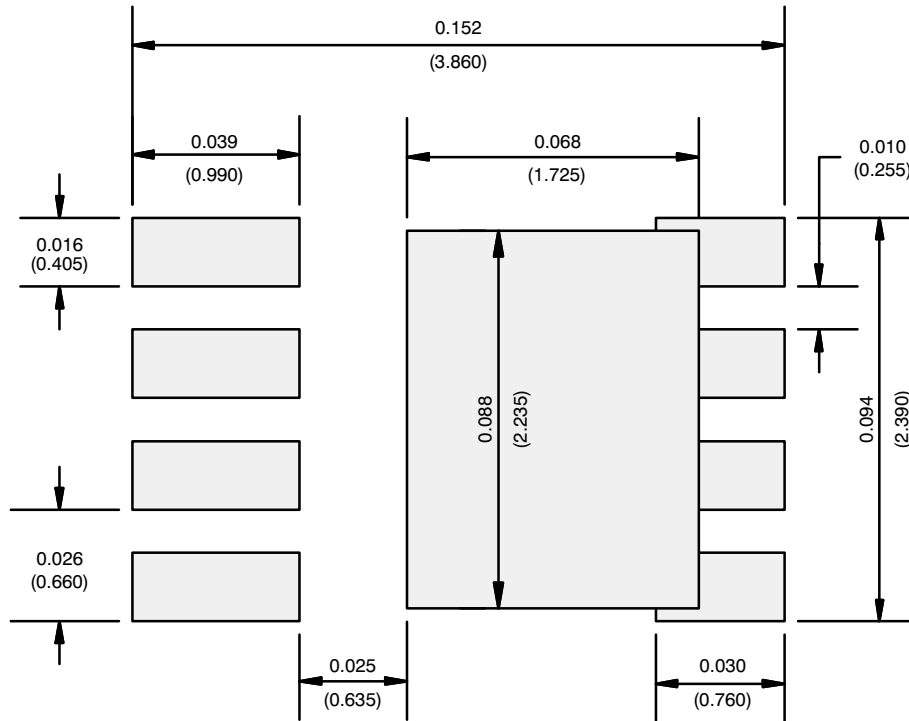
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PowerPAK® 1212-8W Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0	-	0.05	0	-	0.002
A2	0	-	0.13	0	-	0.005
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D4	0.47 typ.			0.0185 typ.		
D5	2.3 typ.			0.090 typ.		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.34 typ.			0.013 typ.		
e	0.65 BSC.			0.026 BSC		
K	0.86 typ.			0.034 typ.		
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
theta	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: C15-1530-Rev. B, 16-Nov-15						
DWG: 6032						

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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