Low V_{IN}, Quad µModule Regulator with Configurable 10A Output Array

FEATURES

- **Quad Output Step-Down µModule Regulator with 10A per Output**
- Input Voltage Range: 2.25V to 5.5V
- Output Voltage Range: 0.5V to V_{IN}
- 10A DC Output Current Each Channel
- Ultra Low EMI Noise
- Parallelable for Up to 40A Output Current
- Selectable Pulse-Skipping Mode/Forced Continuous Mode
- Output Voltage Tracking
- Die Temperature Monitoring Output
- External Frequency Synchronization
- Power Good Indicator
- Overvoltage, Overcurrent and Overtemperature Protection
- 7.5mm × 15mm × 4.65mm BGA Package

APPLICATIONS

- Telecom, Networking and Industrial Equipment
- Multirail Point-of-Load Regulation
- FPGAs, DSPs and ASICs Applications

All registered trademarks and trademarks are the property of their respective owners.

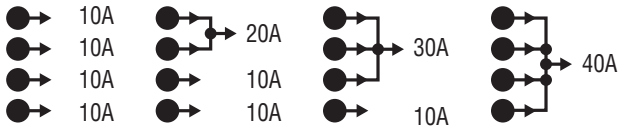
DESCRIPTION

The LTM®4670 is a quad DC/DC step-down µModule® (micromodule) regulator with 10A per output. Outputs can be paralleled in an array for up to 40A capability. Included in the package are the switching controller, power MOSFETs, inductor and all support components. Operating over an input voltage range of 2.25V to 5.5V, each output voltage ranges from 0.5V to V_{IN} set by only one external resistor. Its high efficiency design delivers 10A continuous output current per channel. Only a few input and output capacitors are needed.

The LTM4670 employs a Silent Switcher®2 architecture with internal hot loop bypass capacitors to achieve both low EMI and high efficiency. The default frequency is internally set to 2MHz, it can be externally synchronized to a clock from 1MHz to 2.6MHz.

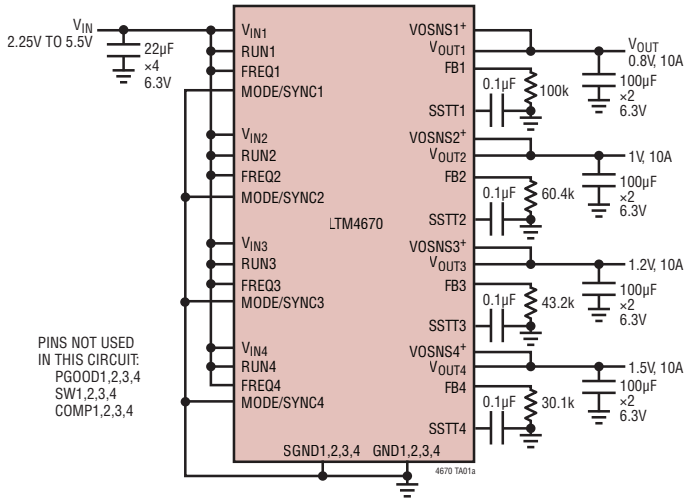
Fault protection features include overvoltage, overcurrent and overtemperature protection. The LTM4670 is Pb-free and RoHS compliant.

Configurable Output Array

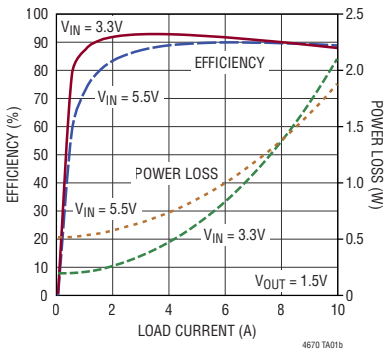


TYPICAL APPLICATION

Quad Output, 10A DC/DC µModule Regulator



Efficiency and Power Loss at 1.5V_{OUT}

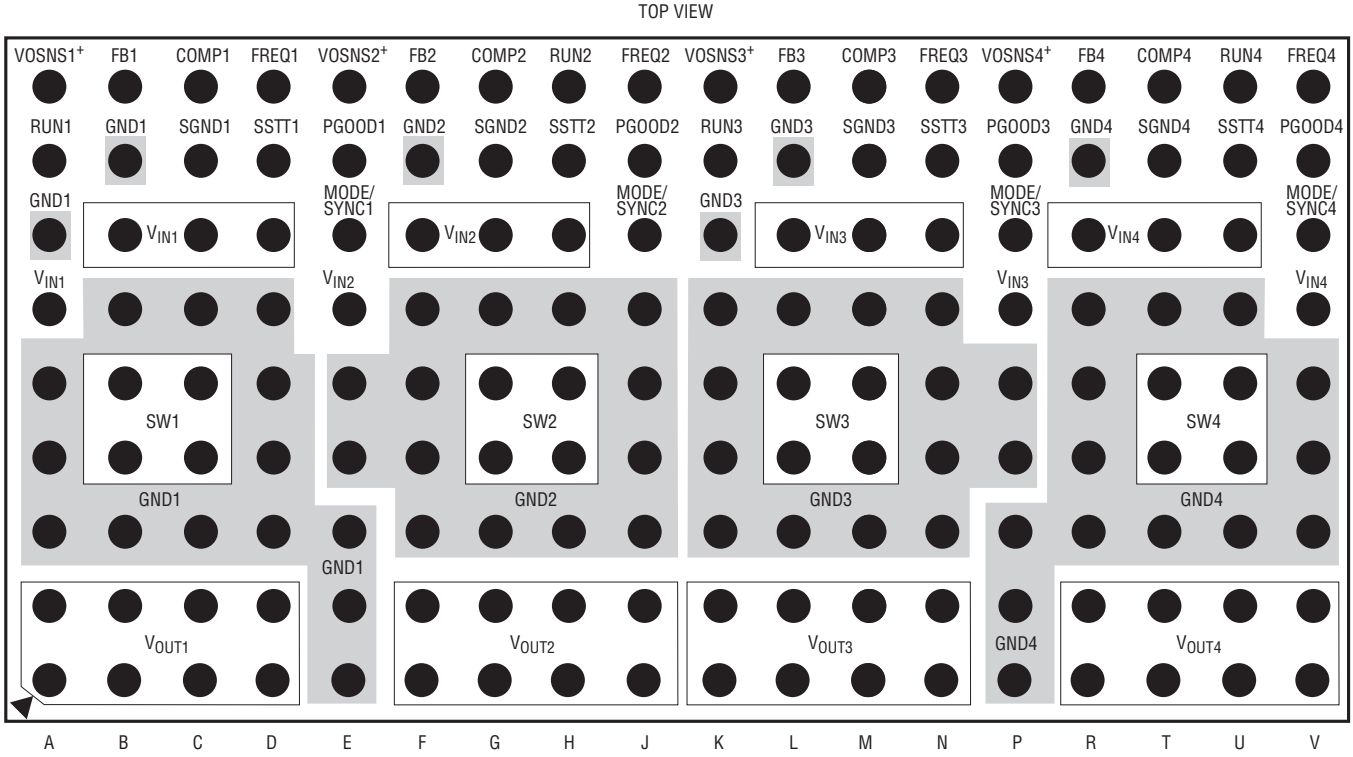


ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN} (per Channel) ..... –0.3V to 6V
V_{OUT}, VOSNS+ (per Channel)..... –0.3V to V_{IN}
RUN, COMP, SSTT, MODE/SYNC, FB,
FREQ, PGOOD (per Channel)..... –0.3V to V_{IN}

Operating Junction Temperature
(Note 2)..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Body Temperature ..... 245°C

PIN CONFIGURATION (See Pin Functions and Table 9)



BGA PACKAGE
162-PIN (15mm × 7.50mm × 4.65mm)
T_{JMAX} = 125°C, θ_{JA} = 9.3°C/W, θ_{JCTOP} = 18.9°C/W, θ_{JCBOT} = 2.5°C/W, WEIGHT = 1.4g

NOTES:
1. θ VALUES ARE DETERMINED BY SIMULATION PER JESD-51 CONDITIONS.
2. θ_{JA} VALUE IS OBTAINED WITH DEMO BOARD.
3. REFER TO APPLICATIONS INFORMATION SECTION FOR LAB MEASUREMENT AND DE-RATING INFORMATION.

ORDER INFORMATION

PART NUMBER	PACKAGE TYPE	BALL FINISH	PART MARKING		MSL RATING	TEMPERATURE RANGE (NOTE 2)
			DEVICE	FINISH CODE		
LTM4670EY#PBF	BGA	SAC305 (RoHS)	LTM4670Y	e1	4	–40°C to 125°C
LTM4670IY#PBF	BGA	SAC305 (RoHS)	LTM4670Y	e1	4	–40°C to 125°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- BGA Package and Tray Drawings
- This product is not recommended for second side reflow. This product is moisture sensitive. For more information, go to Recommended BGA PCB Assembly and Manufacturing Procedures.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C, V_{IN} = 3.3V, per the typical application.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Per Channel							
V_{IN}	Input DC Voltage		●	2.25		5.5	V
$V_{OUT(RANGE)}$	Output Voltage Range		●	0.5		5.5	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	MODE/SYNC = GND, FREQ = V_{IN} (Note 3)	 ●	1.485 1.474		1.515 1.526	V V
V_{IN_UVLO}	V_{IN} Undervoltage Lockout	V_{IN} Rising		2.0	2.1	2.2	V
$V_{IN\_UVLO\_HYS}$	V_{IN} Undervoltage Lockout Hysteresis				150		mV
V_{RUN}	RUN Pin On-Threshold	V_{RUN} Rising		0.375	0.4	0.425	V
V_{RUN_HYS}	RUN Pin Hysteresis				60		mV
I_{RUN}	RUN Pin Leakage Current	RUN = 0.4V				±20	nA
$I_{Q(VIN)}$	Input Supply Bias Current Pulse-Skipping Mode Forced Continuous Mode Shutdown	 V_{OUT} = 1.5V, MODE/SYNC = FREQ = V_{IN} V_{OUT} = 1.5V, MODE/SYNC =0V, FREQ = V_{IN} RUN = 0V (Note 4)		 	 1.7 70 2	 	 mA mA µA
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN} = 3.3V, V_{OUT} = 1.5V (Note 3)				10	A
$\Delta V_{OUT(LINE)}/V_{OUT}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} = 2.5V to 5V, I_{OUT} = 0A				0.3	%/V
$\Delta V_{OUT(LOAD)}/V_{OUT}$	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 10A (Note 3) V_{OUT} = 1.5V, I_{OUT} = 0A to 8A	 ●		0.5 0.2	1.75 1.5	% %
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF + 22µF ×3, V_{IN} = 3.3V, V_{OUT} = 1.5V (Note 4)			12		mV
$\Delta V_{OUT(START)}$	Turn-On Overshoot	I_{OUT} = 0A, C_{OUT} = 100µF + 22µF ×3, V_{IN} = 3.3V, V_{OUT} = 1.5V (Note 4)			5		mV
t_{START}	Turn-On Time	C_{OUT} = 100µF + 22µF ×3, No Load, SSTT = 0.1µF, V_{IN} = 3.3V, V_{OUT} = 1.5V (Note 4)			4.5		ms
I_{SSTT}	Track Pin Soft-Start Pull-Up Current	V_{SSTT} = 0.5V		8	11	14	µA
V_{TEMP} Monitor at 25°C (V_{SSTT})					1.2		V
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 100µF + 22µF ×3, V_{IN} = 3.3V, V_{OUT} = 1.5V (Note 4)			167		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 100µF + 22µF ×3, V_{IN} = 3.3V, V_{OUT} = 1.5V (Note 4)			15		µs
I_{OUTPK}	Output Current Limit	V_{IN} = 3.3V, V_{OUT} = 1.5V			17		A
V_{FB}	Voltage at V_{FB} Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.495	0.50	0.505	V
I_{FB}	Current at V_{FB} Pin					±20	nA
$t_{ON(MIN)}$	Minimum On-Time	(Note 4)			45		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C, V_{IN} = 3.3V, per the typical application.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PGOOD Threshold/ HYS	PGOOD Rising Threshold	As a Percentage of Regulated V_{OUT} (Note 4)			98		%
	PGOOD Hysteresis				1.2		%
	Overvoltage Rising Threshold			105	110	115	%
	Overvoltage Hysteresis			1	2.5	3.5	%
f_{OSC}	Oscillator Frequency	FREQ = V_{IN}		1.8	2	2.2	MHz
MODE/SYNC_RANGE	Sync Frequency Range	FREQ = V_{IN}		1.2		2.6	MHz
MODE/SYNC_LEVEL	Clock Level High on SYNC Clock Level Low on SYNC			1.2		 0.4	V V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

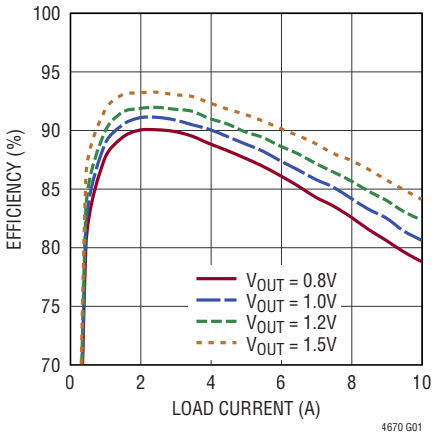
Note 2: The LTM4670 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4670E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4658I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: See output current derating curves for different V_{IN}, V_{OUT} and T_A. Due to the contact resistance and inductance of the test hardware, load regulation results would be better when part is soldered down on the demo board.

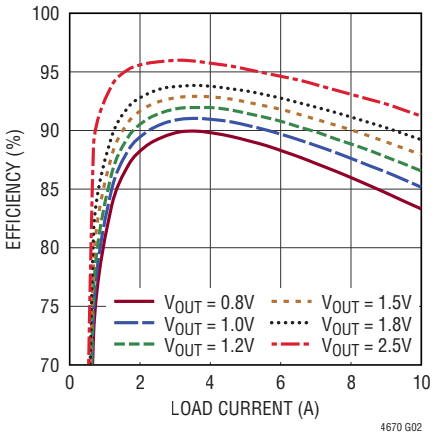
Note 4: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

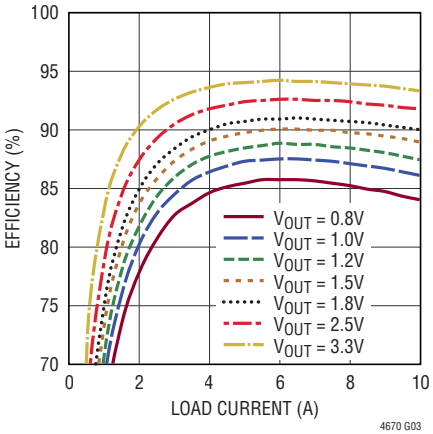
Efficiency vs Load Current, V_{IN} = 2.5V



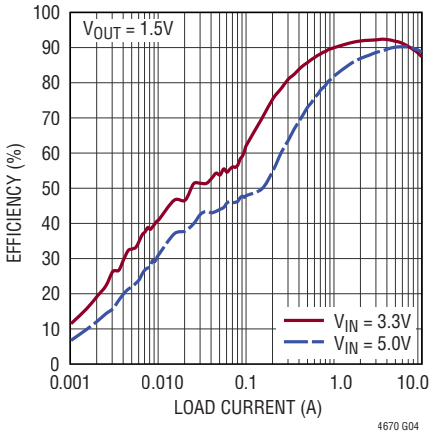
Efficiency vs Load Current, V_{IN} = 3.3V



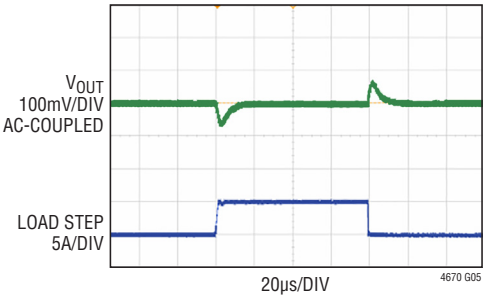
Efficiency vs Load Current, V_{IN} = 5.5V



Pulse-Skipping Mode Efficiency

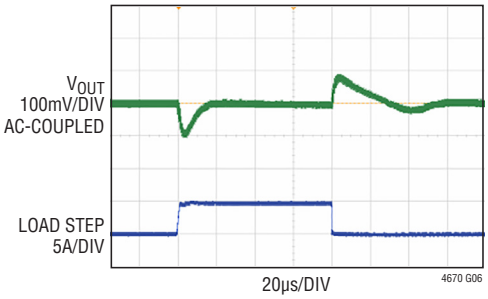


1.0V Output Transient Response



V_{IN} = 3.3V, V_{OUT} = 1.0V, f_{SW} = 2MHz
C_{OUT} = 100µF + 22µF ×3 CERAMIC CAPACITOR
INTERNAL COMPENSATION
C_{FF} = 10pF
0A ~ 5A (50%) LOAD STEP

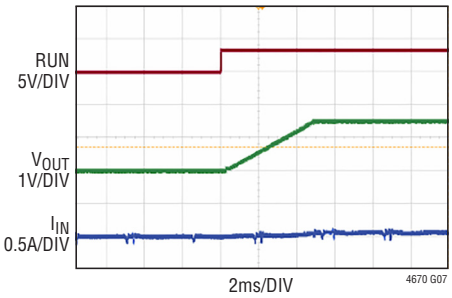
1.5V Output Transient Response



V_{IN} = 3.3V, V_{OUT} = 1.5V, f_{SW} = 2MHz
C_{OUT} = 100µF + 22µF ×3 CERAMIC CAPACITOR
INTERNAL COMPENSATION
C_{FF} = 10pF
0A ~ 5A (50%) LOAD STEP

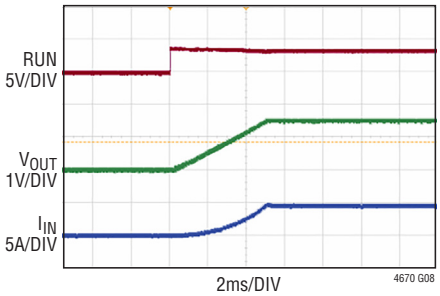
TYPICAL PERFORMANCE CHARACTERISTICS

Start-Up with No Load



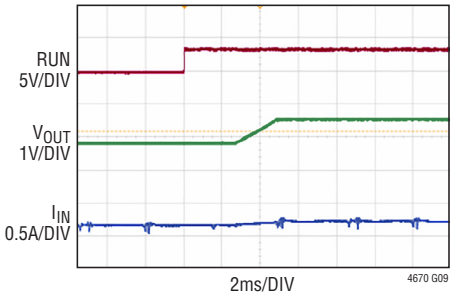
V_{IN} = 3.3V, V_{OUT} = 1.5V, f_{SW} = 2MHz
C_{OUT} = 100µF + 22µF ×3 CERAMIC CAPACITOR

Start-Up with 10A Load



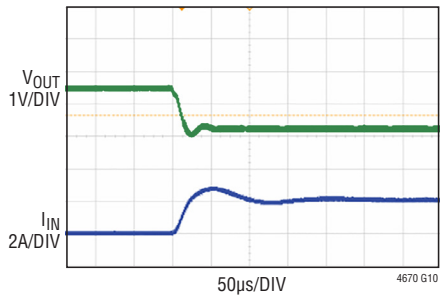
V_{IN} = 3.3V, V_{OUT} = 1.5V, f_{SW} = 2MHz
C_{OUT} = 100µF + 22µF ×3 CERAMIC CAPACITOR

Start Into Prebiased Output



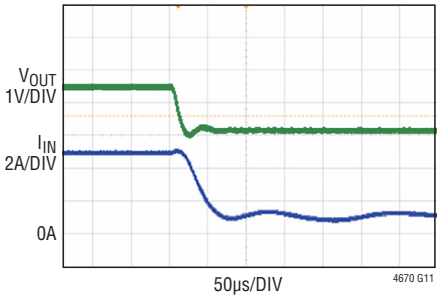
V_{IN} = 3.3V, V_{OUT} = 1.5V, f_{SW} = 2MHz
C_{OUT} = 100µF + 22µF ×3 CERAMIC CAPACITOR

Short-Circuit with No Load Current Applied



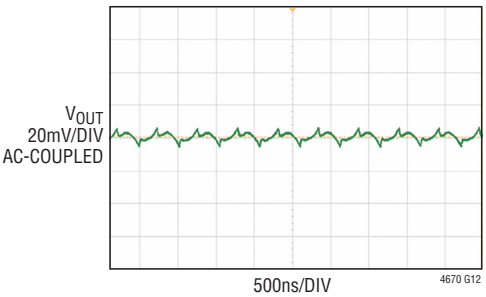
V_{IN} = 3.3V, V_{OUT} = 1.5V, f_{SW} = 2MHz
C_{OUT} = 100µF + 22µF ×3 CERAMIC CAPACITOR
C_{FF} = 10pF

Short-Circuit with 10A Load



V_{IN} = 3.3V, V_{OUT} = 1.5V, f_{SW} = 2MHz
C_{OUT} = 100µF + 22µF ×3 CERAMIC CAPACITOR
C_{FF} = 10pF

Steady State Voltage Ripple



V_{IN} = 3.3V, V_{OUT} = 1.5V, f_{SW} = 2MHz
C_{OUT} = 100µF + 22µF ×3 CERAMIC CAPACITOR
C_{FF} = 10pF

PIN FUNCTIONS

V_{OUT1} (A1, A2, B1, B2, C1, C2, D1, D2), V_{OUT2} (F1, F2, G1, G2, H1, H2, J1, J2), V_{OUT3} (K1, K2, L1, L2, M1, M2, N1, N2), V_{OUT4} (R1, R2, T1, T2, U1, U2, V1, V2): Power Output Pins of the Each Switching Mode Regulator. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins.

GND1 (A3-A5, A7, B3, B6, B8, C3, C6, D3-D6, E1-E3), GND2 (E4, E5, F3-F6, F8, G3, G6, H3, H6, J3-J6), GND3 (K3-K7, L3, L6, L8, M3, M6, N3-N6, P4, P5), GND4 (P1-P3, R3-R6, R8, T3, T6, U3, U6, V3-V5): Power Ground Pins for Both Input and Output Returns.

RUN1 (A8), RUN2 (H9), RUN3 (K8), RUN4 (U9): Each RUN pin has its precision enable threshold with hysteresis. An external resistor divider, from V_{IN} or from another supply, programs the threshold below which the channel will shut down. If the precision threshold is not used, directly connect the pin to V_{IN}. When the RUN pin is low, the channel enters a low current shutdown mode where all internal circuitry is disabled.

VOSNS1$^+$ (A9), VOSNS2$^+$ (E9) VOSNS3$^+$ (K9), VOSNS4$^+$ (P9): Output Voltage Sense Pin of Each Switching Mode Regulator Channel. Internally, this pin is connected to FB pin with a 60.4k precision resistor so only a R_{BOT} is needed to set the output voltage as shown in the Block Diagram in Figure 1. An external divider on FB can be used to set the output voltage if VOSNS$^+$ pin is left open. In multi-phase application, VOSNS$^+$ pins need to be left open for the subordinate channels so FB pins can be tied high. (See the Applications Information section for details.)

SW1 (B4, B5, C4, C5), SW2 (G4, G5, H4, H5), SW3 (L4, L5, M4, M5), SW4 (T4, T5, U4, U5): Switching Node that is used to provide Internal High Current Path from MOSFET to Inductor. Connect with solid cooper area or leave it floating.

V_{IN1} (B7, C7, D7), V_{IN2} (F7, G7, H7), V_{IN3} (L7, M7, N7), V_{IN4} (R7, T7, U7): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

FB1 (B9), FB2 (F9), FB3 (L9), FB4 (R9): The Negative Input of the Error Amplifier. The LTM4670 regulates the voltage between FB and SGND to 500mV. Internally, this pin is connected to VOSNS$^+$ with a 60.4k precision resistor. Different output voltages can be programmed with an additional resistor between V_{FB} and SGND. In PolyPhase® operation, tying the FB pins to V_{IN} to disable the internal Error Amplifier. See the Applications Information section for details.

SGND1 (C8), SGND2 (G8), SGND3 (M8), SGND4 (T8): The SGND pin is the ground reference for the internal analog circuitry, including the bandgap voltage reference. To achieve good load regulation, connect the SGND pin to the negative terminal of the output capacitor (C_{OUT}) at the load. A drop in the high current power ground return path will be compensated. All of the signal components, such as the FB resistor dividers and soft-start capacitor, should be referenced to the SGND node. The SGND node carries very little current and, therefore, can be a minimal size trace.

COMP1 (C9), COMP2 (G9), COMP3 (M9), COMP4 (T9): Current Control Threshold and Error Amplifier Compensation Point of the Switching Mode Regulator Channel. The current comparator's trip threshold is linearly proportional to this voltage. Tie the COMP pins together for parallel operation. The device is internally compensated.

PIN FUNCTIONS

SSTT1 (D8), SSTT2 (H8), SSTT3 (N8), SSTT4 (U8): Soft-Start, Tracking and Temperature Monitor Pin. An internal 10µA current into an external capacitor on the soft-start pin programs the output voltage ramp rate during start-up. When SSTT is below 0.5V, the V_{FB} pin voltage will track the SSTT pin voltage. When SSTT is above 0.5V, the tracking function is disabled, the internal reference resumes control of the error amplifier and the SSTT pin servos to a voltage representative of a junction temperature. During shutdown and fault conditions, the SSTT pin is pulled to ground.

FREQ1 (D9), FREQ2 (J9), FREQ3 (N9), FREQ4 (V9): The FREQ pin sets the oscillator frequency with an external resistor to AGND or sets the phasing for multiphase operation. (See Multiphase Operation in Applications Information section).

MODE/SYNC1 (E7), MODE/SYNC2 (J7), MODE/SYNC3 (P7), MODE/SYNC4 (V7): The MODE/SYNC pin facilitates multiphase operation and synchronization to an external clock. Depending on the mode of operation, the MODE/SYNC pin either accepts an input clock pulse or outputs a clock pulse at its operating frequency. (See Multiphase Operation in Applications Information). The MODE/SYNC pin also programs the mode of operation: pulse-skipping or forced continuous.

PGOOD1 (E8), PGOOD2 (J8), PGOOD3 (P8), PGOOD4 (V8): Output Power Good with Open-Drain Logic of the Switching Mode Regulator Channel. PGOOD is pulled to ground when the voltage on the FB pin is not within –2%/+10% of the internal 0.5V reference.

BLOCK DIAGRAM

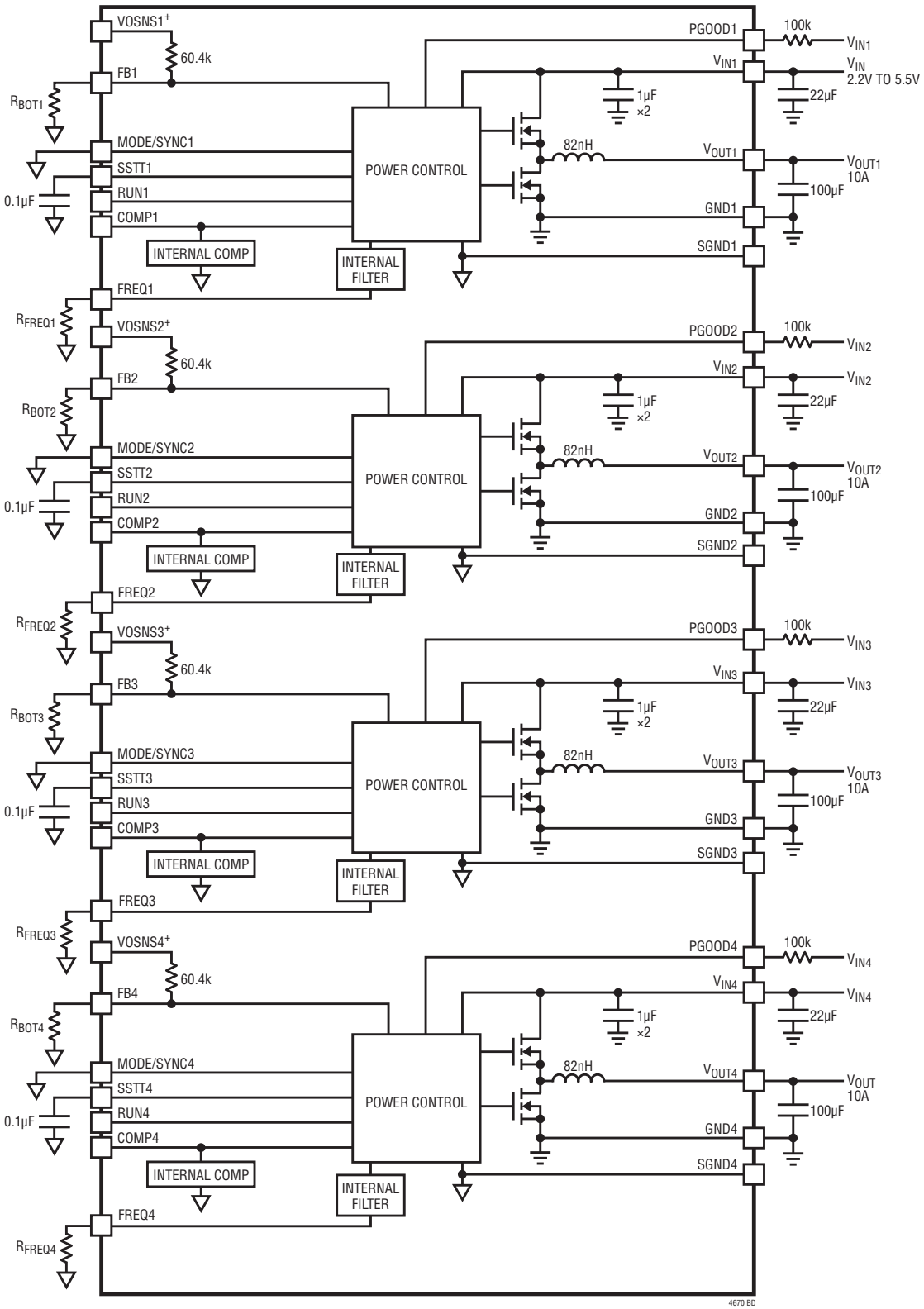


Figure 1. Simplified LTM4670 Block Diagram

DECOUPLING REQUIREMENTS (PER CHANNEL)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement, (V_{IN} = 2.25V to 5.5V, V_{OUT} = 1.5V)	I_{OUT} = 10A	22			µF
C_{OUT}	External Output Capacitor Requirement, (V_{IN} = 2.25V to 5.5V, V_{OUT} = 1.5V)	I_{OUT} = 10A	100			µF

OPERATION

The LTM4670 is a quad output standalone non-isolated switch mode DC/DC power supply. It integrates four separate regulators with each of them capable of delivering up to 10A continuous output current with few external input and output capacitors. Each regulator provides precisely regulated output voltage programmable from 0.5V to V_{IN} via a single resistor over 2.25V to 5.5V input voltage range. The typical application schematic is shown in the front page.

The LTM4670 integrates 4 separate constant frequency peak current mode step-down control regulators with power MOSFETs, inductors, and other supporting discrete components. It employs the second-generation Silent Switcher technology in which it allows fast switching edges for high efficiency at high switching frequencies, while simultaneously achieving good EMI performance. Ceramic capacitors on V_{IN} keep all the fast AC current loops small, improving EMI performance.

Current mode control provides cycle-by-cycle fast current limiting and overcurrent protection. Internal feedback loop compensation provides sufficient stability margins and good transient performance with wide range of output capacitors, even with all ceramic output capacitors.

The default switching frequency for LTM4670 is 2MHz. It can be externally synchronized to a clock from 1.2MHz to 2.6MHz.

Internal undervoltage and overvoltage comparators pull the open-drain PGOOD output low if the output voltage exists a –2/+10% window around the regulation point. Furthermore, in an overvoltage condition, internal top MOSFET is turned off and bottom MOSFET is turn.

For systems with higher power requirements, multiphase operation can be easily employed with the synchronization and phase mode controls.

Pulling the RUN pin to GND forces the regulator into its shutdown state, turning off both power MOSFETs and most of the internal control circuitry. At light load currents, pulse-skipping mode operation can be enabled to achieve higher efficiency. If low output ripple is desired, forced continuous mode can be selected.

The SSTT pin is used for power supply tracking, soft-start programming and monitor die temperature. See the Applications Information

APPLICATIONS INFORMATION

The typical LTM4670 application circuit is shown in the front page. External component selection is primarily determined by the input voltage, the output voltage and the maximum load current. Refer to Table 8 for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Step-Down Ratios

The minimum V_{OUT} step-down ratio that can be achieved for a given input voltage is limited by the minimum on-time.

The minimum on-time limit imposes a minimum duty cycle of the converter which can be calculated with Equation 1.

$$D_{(MIN)} = t_{ON(MIN)} \bullet f_{SW} \quad (1)$$

where $t_{ON(MIN)}$ is the minimum on-time, 45ns typical for LTM4670. In the rare cases where the minimum duty cycle is surpassed, the output voltage will remain in regulation, but the switching frequency will decrease from its programmed value, a slower switching frequency can be used to accommodate a high V_{IN}/V_{OUT} ratio.

The LTM4670 is capable of a maximum duty cycle of 100%, therefore, the V_{IN}-to-V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch, the inductor DCR and the load current.

Output Voltage Programming

The PWM controller has an internal 0.5V reference voltage. As show in the Figure 1 (Block Diagram), a 60.4k internal feedback resistor connects each regulator channel from V_{FB} to $VOSNS^+$ pins which should be directly connected to V_{OUT}. Adding a resistor R_{BOT} from FB pin to SGND pin programs the output voltage (Equation 2)

$$V_{OUT} = 0.5V \bullet \frac{60.4k + R_{BOT}}{R_{BOT}} \quad (2)$$

1% resistors are recommended to maintain output voltage accuracy.

Input Decoupling Capacitors

The LTM4670 module should be connected to a low AC-impedance DC source. For each channel, one-piece 22µF input ceramic capacitor is recommended to place as close as possible to the pins for RMS ripple current decoupling. Bulk input capacitor is only needed when the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. The bulk capacitors can be an electrolytic aluminum capacitor and/or polymer capacitor.

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated with Equation 3.

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)} \quad (3)$$

where $\eta\%$ is the estimated efficiency of the power module and D is the duty cycle.

Output Decoupling Capacitors

With an optimized high frequency, high bandwidth design, only a 100µF ceramic capacitor is required for LTM4670 to achieve low output voltage ripple and very good transient response. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 8 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 5A (50%) load step transient.

Multiphase operation will reduce effective output ripple as a function of the number of phases. Analog Devices Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance will be more of a function of stability and transient response. The Analog Devices LTpowerCAD® design tool is available to download online for output ripple, stability and transient response analysis and calculating the output ripple reduction as the number of phases implemented increases by N times.

Mode of Operation

The MODE/SYNC pin either synchronizes the switching frequency to an external clock, is a clock output, or sets the PWM mode. The PWM modes of operation are either pulse-skipping or forced continuous. See Table 1.

The LTM4670 operates in forced continues mode for low noise or pulse-skipping mode for high efficiency at light load.

APPLICATIONS INFORMATION

The LTM4670 operates in pulse-skipping mode when both the FREQ and MODE/SYNC pins are connected to V_{IN}. In this mode, the switching cycles are skipped at light load to regulate the output voltage. The LTM4670 defaults to forced continuous mode during synchronization.

Table 1. LTM4670 Single Phase Configuration

FREQ PIN CONNECTION	MODE/SYNC PIN CONNECTION	MODE OF OPERATION	SWITCHING FREQUENCY
V_{IN}	Clock Input	Forced Continuous	External Clock
V_{IN}	AGND	Forced Continuous	2MHz Default
V_{IN}	V_{IN}	Pulse-Skipping	2MHz Default
Resistor to AGND	Clock Output	Forced Continuous	FREQ Programmed

Setting the Operating Frequency

The LTM4670 uses a constant frequency PWM architecture. There are three methods to set the switching frequency. The first method is with a resistor (R_{FREQ}) tied from the FREQ pin to ground. The frequency can be programmed to switch from 1.2MHz to 2.6MHz. Table 2 shows the necessary R_{FREQ} value for a desired switching frequency.

The R_{FREQ} resistor required for a desired switching frequency is calculated using E4.

$$R_{FREQ} = 568 \bullet f_{SW}^{(-1.08)} \quad (4)$$

The second method to set the LTM4670 switching frequency is by synchronizing the internal PLL circuit to an external frequency applied to the MODE/SYNC pin. The synchronization frequency range is 1.2MHz to 2.6MHz. The LTM4670 operates in forced continuous mode when synchronized to an external clock.

The third method of setting the LTM4670 switching frequency is to use the internal nominal 2MHz default clock. See Table 1 for pin configuration.

Table 2. SW Frequency vs R_{FREQ} Value

f_{SW} (MHz)	R_{FREQ} (kΩ)
1	549
2	274
2.2	243
3.0	178

Synchronizing the Oscillator to an External Clock

The LTM4670 switching frequency can be adjusted by synchronizing the internal PLL circuit to an external clock to the MODE/SYNC pin. The synchronization frequency range is 1.2MHz to 2.6MHz. The LTM4670 operates in forced continuous mode when synchronize to an external clock. During synchronization, the top power switch turn-on is locked to the rising edge of the external frequency source. The slope compensation is automatically adapted to the external clock frequency.

At start up, before the LTM4670 recognizes the external clock applied to MODE/SYNC, the LTM4670 will switch at its default frequency of 2MHz. Once the externally applied clock is recognized, the switching frequency will gradually transition from the default frequency to the applied frequency. If the external clock is removed, the LTM4670 will slowly transition back to the default frequency.

The synchronizing clock amplitude should be greater than 1.2V and less than 0.4V with a pulse width greater than 40ns. An internal 200k resistor on MODE/SYNC pin to AGND allows the MODE/SYNC to be floating. Please note that low switching frequency will increase the inductor peak current and the output voltage ripple.

Multiphase Operation

For output loads that demand more than 10A of current, multiple LTM4670s can be paralleled to run out of phase to provide more output current without increasing input and output voltage ripples. See Table 3.

Table 3. LTM4670 Multiphase Configuration

MAIN/SUBORDINATE	FREQ PIN	FB PIN	MODE/SYNC PIN	SWITCHING FREQUENCY (f_{SW})
Main	V_{IN}	V_{OUT} Divider	Clock Input	External Clock/2MHz Default
Main	Resistor to AGND	V_{OUT} Divider	Clock Output	FREQ Programmed
Subordinate	V_{IN} Divider	V_{IN}	Clock Input	External Clock

APPLICATIONS INFORMATION

To parallel multiple LTM4670 channels to achieve the same switching frequency, a perfect interleaved phase shift and an accurate current sharing between different channels, one of the LTM4670 will become the main channel and the rest of LTM4670s need to be programmed to be subordinate channels.

1. Connecting a resistor from FREQ to AGND of the main phase will programs the frequency and configures the MODE/SYNC pin to become a clock output used to drive the MODE/SYNC pin of the subordinate phase(s).
2. Connecting the FREQ pin of the main phase to V_{IN} configures the MODE/SYNC pin to become an input capable of accepting an external clock. The switching frequency defaults to the nominal 2MHz internal frequency when the external clock is unavailable, such as during start-up.
3. Connecting the FB pin to V_{IN} configures a phase as subordinate. The MODE/SYNC becomes an input and the voltage control loop is disabled. The subordinate phase current control loop is still active and the peak current is controlled via the shared ITH node. Careful consideration should be taken when routing the ITH node between phases. Routing the ITH and AGND nodes together is recommended to create a low inductance path.
4. Connecting the PGOOD pins together and adding an external pull-up resistor allows the main phase to communicate with the subordinate phases on when start-up has been completed.

Programming Subordinate Phase Angle

The phasing of a subordinate phase relative to the main phase is programmed with a resistor divider from V_{IN} to FREQ pins. See Figure 2 and Table 4 for phase programming. Use of 1% resistors is recommended.

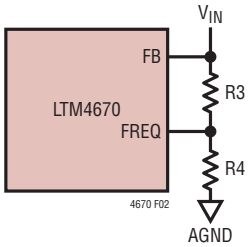


Figure 2. Phase Programming

Table 4. Subordinate Module Phase Shift Related to MODE/SYNC Input

SYNC PHASE ANGLE	R3 RATIO	R4 RATIO	R3 EXAMPLE	R4 EXAMPLE
0°	0Ω	N/A	0Ω	N/A
90°	3 • R	R	301k	100k
120°	7 • R	5 • R	243k	174k
180°	N/A	0Ω	N/A	0Ω
240°	5 • R	7 • R	174k	243k
270°	R	3 • R	100k	300k

When configured for main/subordinate operation, the subordinate phases operate in force continuous modes.

The LTM4670 device is an inherently current mode controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design. Tie RUN, PGOOD, and COMP pins of each paralleling channel together. Figure 17 shows an example of parallel operation and pin connection.

Input RMS Ripple Current Cancellation

A proper interleaving phase in a multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used when all the outputs are tied together to achieve a single high output current design.

Application Note 77 provides detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivation are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number if interleaved phases. Figure 3 shows this graph.

For the LTM4670, all four channels can be configured to run independently providing 4 separate outputs or channels can be paralleled for a multiphase single output operation. To reduce input/output ripples for four independent channels, a multiphase oscillator such as the

APPLICATIONS INFORMATION

LTC6902 can be used to interleave the phase such that all four channels are phase shifted 90 degree from each other (see Figure 16). To achieve low output ripple for the multiphase single output configuration, main/subordinate configuration can also be programmed by the FREQ pin to interleave the phases (see Figure 17).

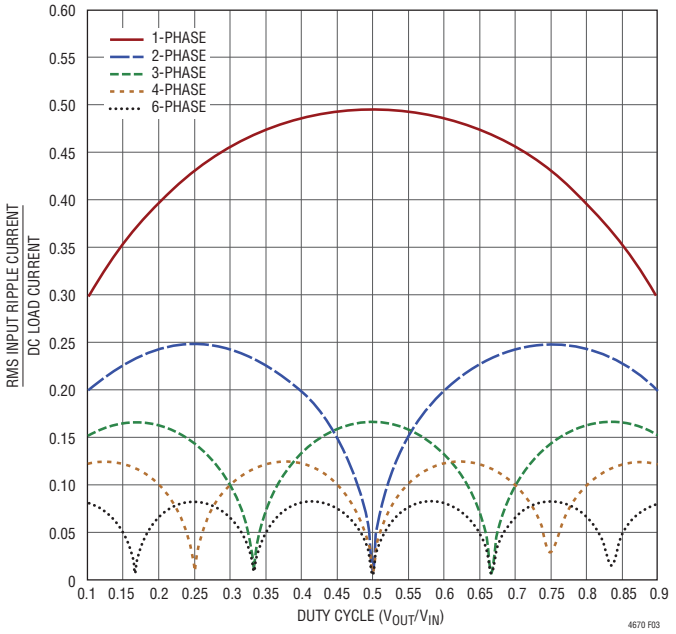


Figure 3. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle

Soft-Start/Tracking/Temperature Monitor

The LTM4670 allows the user to program its output voltage ramp rate by means of the SSTT pin.

An internal 10µA pulls up the SSTT pin. Putting an external capacitor on SSTT enables soft-starting the output to prevent current surge on the input supply and output voltage overshoot. During the soft-start ramp, the output voltage will proportionally track the SSTT pin voltage. When the soft-start is complete, the pin will servo to a voltage proportional to the junction temperature of that channel. See Figure 4 showing the SSTT pin operating range.

The soft-start time is calculated using Equation 5.

$$T_{SS} = C_{SS} \bullet \frac{500mV}{10\mu A} \quad (5)$$

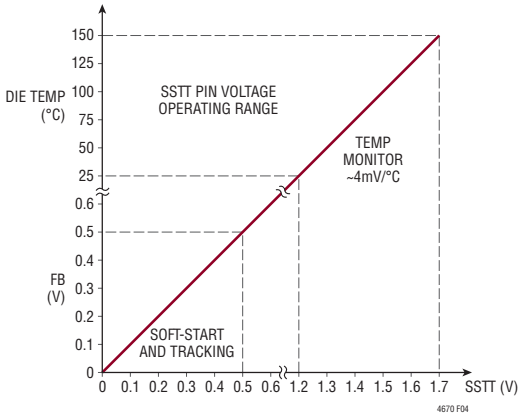


Figure 4. Soft-Start and Temperature Monitor Operation

For output tracking applications, SSTT can be externally driven by another voltage source. From 0V to 0.5V, the SSTT voltage will override the internal 0.5V reference input to the error amplifier, thus regulating the FB pin voltage to that of SSTT pin voltage. When SSTT is above 0.5V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage.

An active pull-down circuit is connected to the SSTT pin to discharge the external soft-start capacitor in the case of fault conditions. The ramp will restart when the fault is cleared. Fault conditions that clear the soft-start capacitor are the RUN pin transitioning low, V_{IN} voltage falling too low or thermal shutdown.

Once the soft-start cycle has completed and the output power good flag thrown, the SSTT pin reports the die junction temperature. The LTM4670 regulates the SSTT pin to a voltage proportional to the junction temperature. While reporting the temperature, the SSTT voltage is not valid below 1V. The junction temperature is calculated with Equation 6.

$$T_J\ (°C) = \frac{V_{SSTT}}{4mV} - 273 \quad (6)$$

The following procedure is used for a more accurate measurement of the junction temperature:

1. Measure the ambient temperature T_A.

APPLICATIONS INFORMATION

2. Measure the SSTT voltage while in pulse-skipping mode with the V_{OUT} pulled up slightly higher than the regulated V_{OUT}.
3. Calculate the slope of the temperature sensing circuit using Equation 7.

$$\text{Slope (mV / °C)} = \frac{V_{SSTT}}{T_A + 273} \quad (7)$$

4. Calculate the junction temperature with the new calibrated slope.

When the output voltage goes out of regulation and the power good pin is pulled low, the soft-start pin no longer reports the temperature.

During multiphase operation, the soft-start feature of the subordinate channels is disabled and the SSTT pin can be left floating. However, a small capacitor can be still placed from SSTT pin to AGND for better junction temperature readings.

Power Good

The PGOOD pins are open-drain pins that can be used to monitor valid output voltage regulation. This pin monitors a –2/+10% window around the regulation point. A resistor can be pulled up to a particular supply voltage for monitoring. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTM4670's PGOOD falling edge includes a blanking delay of approximately 100µs. The PGOOD is also actively pulled low during fault conditions: RUN pin is low, V_{IN} is too low or in thermal shutdown.

For multiphase applications the PGOOD pin is used for communication between the main and subordinate phases.

Connect the PGOOD pins together and pull-up to V_{IN} or V_{OUT} with an external resistor.

Stability Compensation

The LTM4670 module internal compensation loop is designed and optimized for low ESR ceramic output capacitors. Table 8 is provided for most application requirements. In case a bulk output capacitor is required for output ripple or dynamic transient spike reduction, an additional 10pF to 15pF phase feedforward capacitor (C_{FF}) is needed between V_{OUT} and FB. The LTpowerCAD Design Tool is available to download for control loop optimization.

RUN Enable

Each channel of the LTM4670 has its precision threshold RUN pin to enable or disable the switching for each channel. When forced low, the RUN pin puts the channel into a low current shutdown mode. The rising threshold of the RUN comparator is 400mV, with 60mV of hysteresis. It can be tied to V_{IN} if the shutdown feature is not used. Adding a resistor divider from V_{IN} to RUN programs the LTM4670 to regulate the output only when V_{IN} is above a desired voltage. Typically, this threshold, $V_{IN(RUN)}$, is used in situations where the input supply is current limited or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(RUN)}$ threshold prevents the regulator from operating at source voltages where problems may occur. This threshold can be adjusted by setting the values R1 and R2 such that they satisfy Equation 8.

$$V_{IN(RUN)} = \left(\frac{R1}{R2} + 1\right) \bullet 400mV \quad (8)$$

where the LTM4670 will remain off until V_{IN} is above $V_{IN(RUN)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below $V_{IN(RUN)}$.

Alternatively, a resistor divider from an output of another channel to the RUN pin of the LTM4670 provides event-based power-up sequencing, enabling the LTM4670 when the output of the other regulator reaches a predetermined level.

Output Short-Circuit Protection and Recovery

The peak inductor current level, at which the current comparator shuts off the top power switch, is controlled by the COMP voltage. When the output current increases, the error amplifier raises COMP voltage until the average inductor current matches the load current. There is a clamp set for the COMP voltage, thereby setting the current limit.

APPLICATIONS INFORMATION

When the output is shorted to ground, the inductor current decays very slowly during a single switching cycle because the voltage across the inductor is low. To keep the inductor current in control, a secondary limit is imposed on the valley of the inductor current. If the inductor current measured through the bottom power switch is greater than the $I_{VALLEY(MAX)}$, the top power switch will be held off. Subsequent switching cycles will be skipped until the inductor current falls below $I_{VALLEY(MAX)}$.

Recovery from a short circuit can be abrupt because when the output is shorted and below the regulation point, the regulator is requesting the maximum current to recharge the output. This inductor current could cause an extreme voltage overshoot in the output when the short circuit condition is removed. The LTM4670 addresses this potential issue by regulating the SSTT pins voltage above the FB voltage anytime the output is out of regulation. Therefore, a recovery from an output short circuit goes through a soft-start cycle to control the output ramp and the overshoot is minimized.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board. The motivation for providing these thermal coefficients in found in JESD51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are, in-and-of themselves, not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

- θ_{JA}, the thermal resistance from junction-to-ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a demo board DC2891A.
- $\theta_{JCbottom}$, the thermal resistance from junction to bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical module regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value maybe useful for comparing packages but the test conditions don't generally match the user's application.
- θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

A graphical representation of the aforementioned thermal resistances is given in Figure 5; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule.

APPLICATIONS INFORMATION

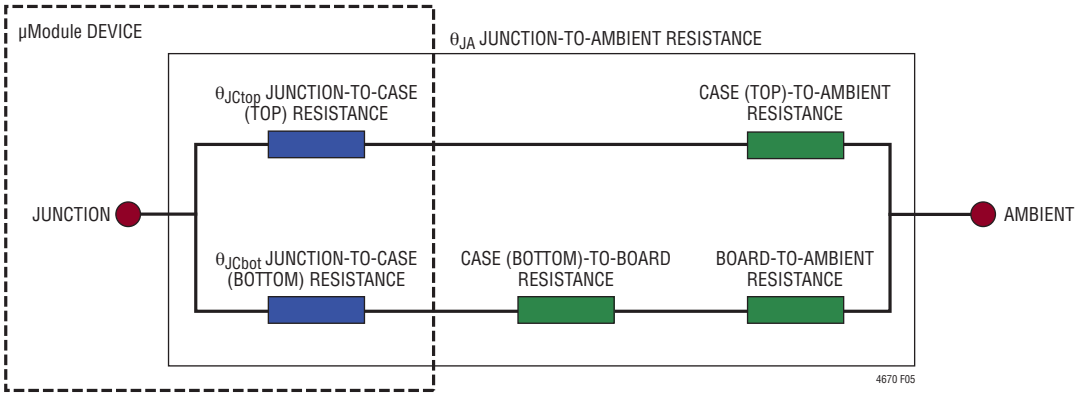


Figure 5. Graphical Representation of Thermal Coefficients, Including JESD51-12 Terms

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

The SSTT pins can provide the junction temperature reading of each channel within the module. Within the LTM4670 module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JSED51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4670 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due-diligence yields a set of derating curves shown in this data sheet.

The power loss curves in Figure 6, Figure 7 and Figure 8 can be used in coordination with the load current derating curves in Figure 9 to Figure 14 for calculating an approximate θ_{JA} thermal resistance for the LTM4670 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with multiplicative factors according to the junction temperature. This approximate factor is: 1.2 for 120°C at junction temperature. Maximum load current is achievable while increasing ambient temperature as long as the junction temperature is less than 120°C, which is 5°C guard band from maximum junction temperature of 125°C. When the ambient temperature reaches a point

APPLICATIONS INFORMATION

where the junction temperature is 120°C, then the load current is lowered to maintain the junction at 120°C while increasing ambient temperature up to 120°C. The derating curves are plotted with the output current starting at 40A and the ambient temperature at 30°C. The output voltages are 0.6V, 1.0V, 1.8V and 3.3V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. For example, to determine the maximum ambient temperature when each channel is running at V_{IN} = 3.3V, V_{OUT} = 1.5V and 5A load current without a heat sink and 400LFM airflow, simply add up the total power loss for each channel from Figure 7 which equals to 2.56W in this case, then multiply by the 1.2 coefficient for 120°C junction temperature, the total power loss for 4 channels is 3.07W, If the 94.4°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 25.6°C divided by 3.07W equals a 8.3°C/W for θ_{JA} the system equivalent thermal resistance. Table 6 specifies 8.5°C/W value which is very close. Table 5 and Table 7 provide equivalent thermal resistances for 1V and 2.5V outputs with and without airflow. The derived thermal resistances in Table 5 to Table 7 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above temperature multiplicative factors. The referenced printed circuit board is a 1.6mm thick 6-layer board with two-ounce copper for the two outer layers and one-ounce copper for the two inner layers. The PCB dimensions are 106mm × 104mm.

APPLICATIONS INFORMATION

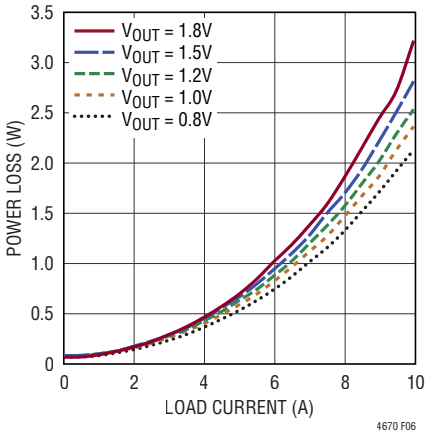


Figure 6. Power Loss vs Load Current at $2.5V_{IN}$

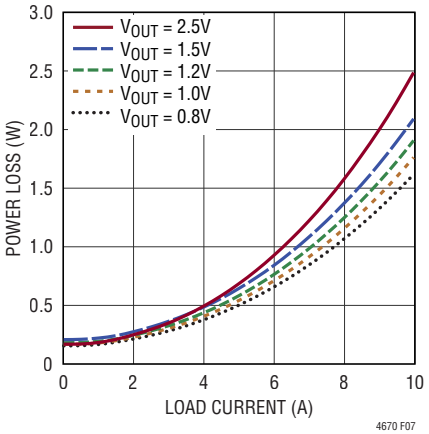


Figure 7. Power Loss vs Load Current at $3.3V_{IN}$

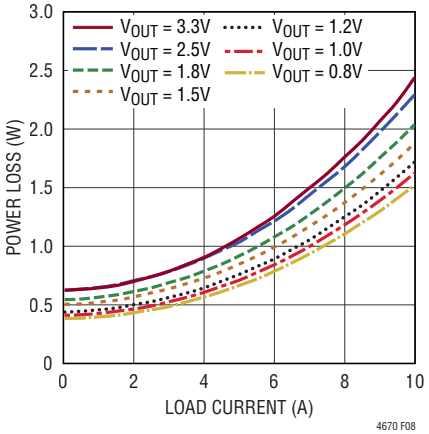


Figure 8. Power Loss vs Load Current at $5.5V_{IN}$

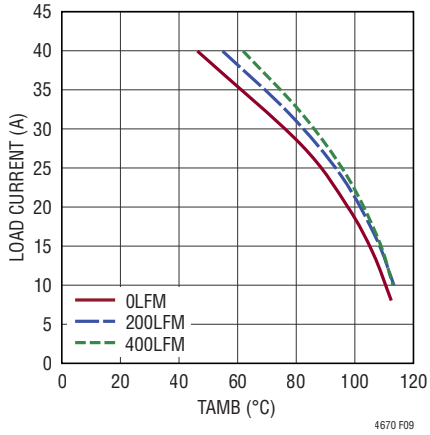


Figure 9. 3.3V to 1V Derating Curve, No Heat Sink

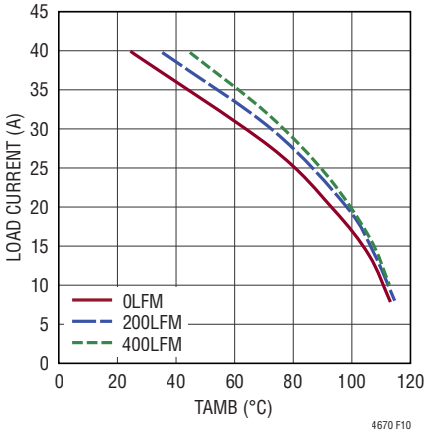


Figure 10. 3.3V to 1.5V Derating Curve, No Heat Sink

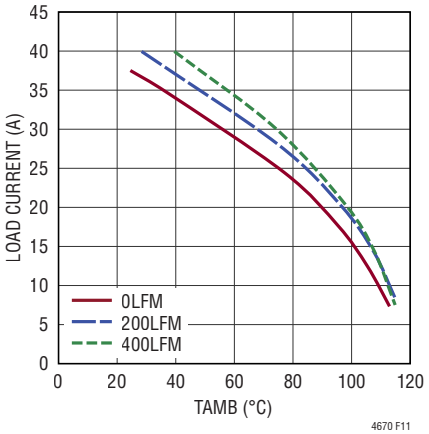


Figure 11. 3.3V to 2.5V Derating Curve, No Heat Sink

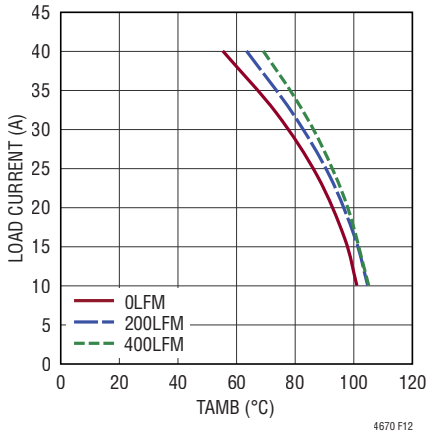


Figure 12. 5V to 1.0V Derating Curve, No Heat Sink

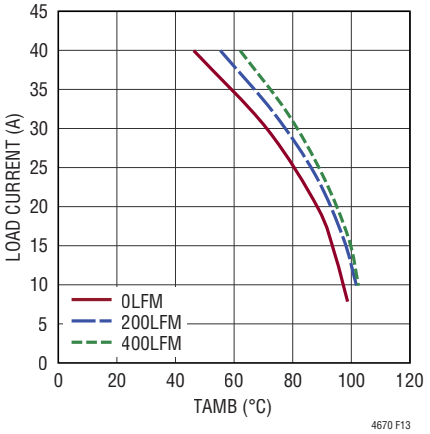


Figure 13. 5V to 1.5V Derating Curve, No Heat Sink

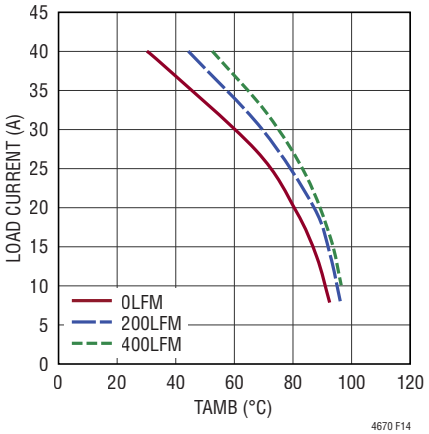


Figure 14. 5V to 2.5V Derating Curve, No Heat Sink

APPLICATIONS INFORMATION

Table 5. 1.0V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 9, Figure 12	3.3, 5.5	Figure 6, Figure 7, Figure 8	0	None	8.6
Figure 9, Figure 12	3.3, 5.5	Figure 6, Figure 7, Figure 8	200	None	7.4
Figure 9, Figure 12	3.3, 5.5	Figure 6, Figure 7, Figure 8	400	None	6.7

Table 6. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 10, Figure 13	3.3, 5.5	Figure 6, Figure 7, Figure 8	0	None	8.5
Figure 10, Figure 13	3.3, 5.5	Figure 6, Figure 7, Figure 8	200	None	7.6
Figure 10, Figure 13	3.3, 5.5	Figure 6, Figure 7, Figure 8	400	None	6.7

Table 7. 2.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 11, Figure 14	3.3, 5.5	Figure 6, Figure 7, Figure 8	0	None	9.1
Figure 11, Figure 14	3.3, 5.5	Figure 6, Figure 7, Figure 8	200	None	7.6
Figure 11, Figure 14	3.3, 5.5	Figure 6, Figure 7, Figure 8	400	None	6.8

Table 8. Output Voltage Response vs Component Matrix (Refer to Front Page Application Circuit) 0A to 5A Load Step Typical Measured Values

C_{IN} BULK VENDORS	PART NUMBER	DESCRIPTION	C_{IN} CERAMIC VENDORS	PART NUMBER	DESCRIPTION	C_{OUT} CERAMIC VENDORS	PART NUMBER	DESCRIPTION
PANASONIC	10SVP150MX	150µF, 10V	AVX	0603ZD226MAT2A	22µF, 10V	KEMET	C0805C226M9PACTU	22µF, 6.3V
			SAMSUNG	CL10A475KP8NNNC	4.7µF, 10V	MURATA	GRM21BR60J107ME15K	100µF, 6.3V

V_{OUT} (V)	C_{IN} (CERAMIC)	C_{IN} (BULK)	$C_{OUT1,2,3,4}$ (CERAMIC)	C_{FF} (pF)	V_{IN} (V)	DROOP (mV)	P-P DERIVATION (mV)	RECOVERY TIME (µs)	LOAD STEP (A)	LOAD STEP SLEW RATE (A/µs)	R_{FB} (kΩ)
0.8	22µF ×5 + 4.7µF ×2	150µF	22µF ×3 + 100µF	10	3.3	70	144	10	5	5	100
0.8	22µF ×5 + 4.7µF ×2	150µF	22µF ×3 + 100µF	10	5	70	147	10	5	5	100
1.0	22µF ×5 + 4.7µF ×2	150µF	22µF ×3 + 100µF	10	3.3	80	157	10	5	5	60.4
1.0	22µF ×5 + 4.7µF ×2	150µF	22µF ×3 + 100µF	10	5	80	161	10	5	5	60.4
1.5	22µF ×5 + 4.7µF ×2	150µF	22µF ×3 + 100µF	10	3.3	90	181	15	5	5	30.1
1.5	22µF ×5 + 4.7µF ×2	150µF	22µF ×3 + 100µF	10	5	90	184	15	5	5	30.1
1.8	22µF ×5 + 4.7µF ×2	150µF	22µF ×3 + 100µF	10	3.3	100	203	15	5	5	23.2
1.8	22µF ×5 + 4.7µF ×2	150µF	22µF ×3 + 100µF	10	5	100	206	15	5	5	23.2
2.5	22µF ×5 + 4.7µF ×2	150µF	22µF ×3 + 100µF	10	3.3	130	258	15	5	5	15
2.5	22µF ×5 + 4.7µF ×2	150µF	22µF ×3 + 100µF	10	5	130	258	15	5	5	15
3.3	22µF ×5 + 4.7µF ×2	150µF	22µF ×3 + 100µF	10	5	160	325	15	5	5	10.7

APPLICATIONS INFORMATION

Safety Considerations

The LTM4670 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and over current protection.

Layout Checklist/Example

The high integration of LTM4670 makes the PCB board layout very simple and easy. However to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND1,2,3,4 underneath the unit.
- For parallel modules, tie the V_{OUT}, RUN, COMP, and PGOOD pins from each phase together. Use an internal layer to closely connect these pins together.
- Bring out test points on the signal pins for monitoring.

Figure 15 gives a good example of the recommended layout.

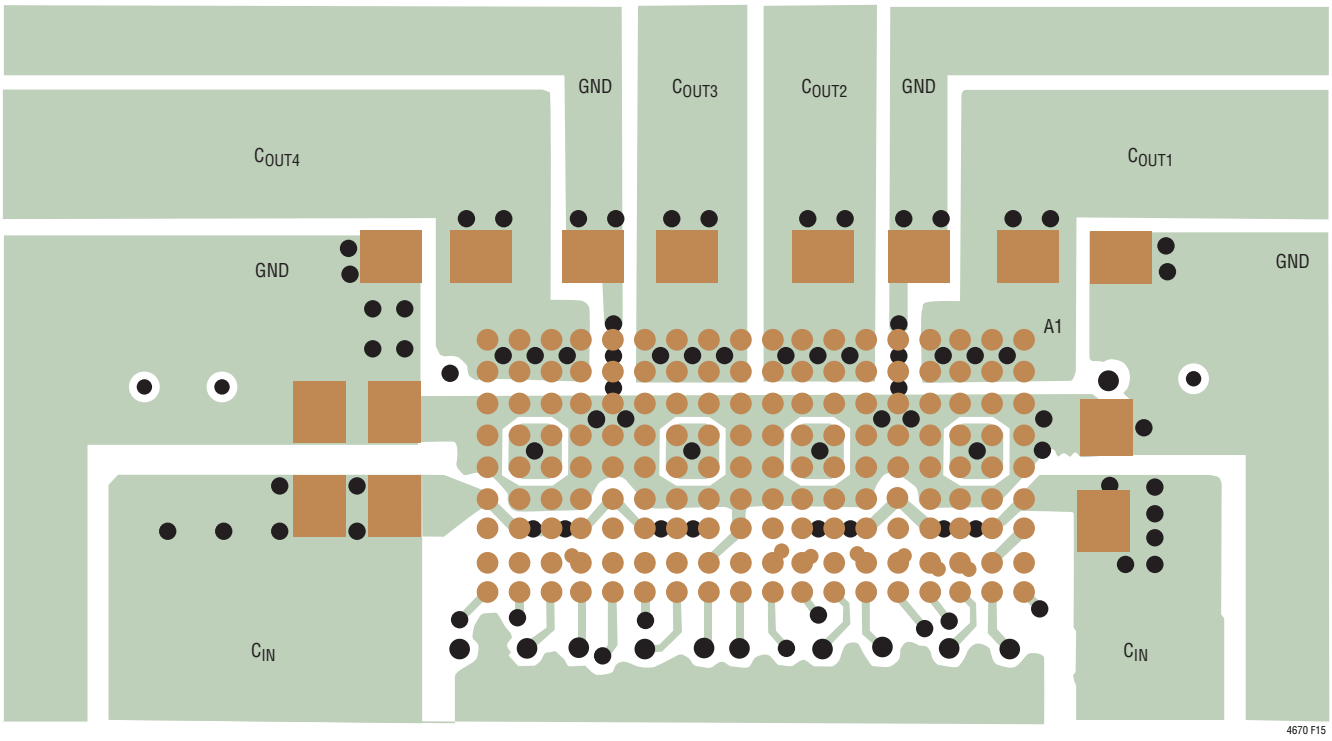


Figure 15. Recommended PCB Layout

TYPICAL APPLICATIONS

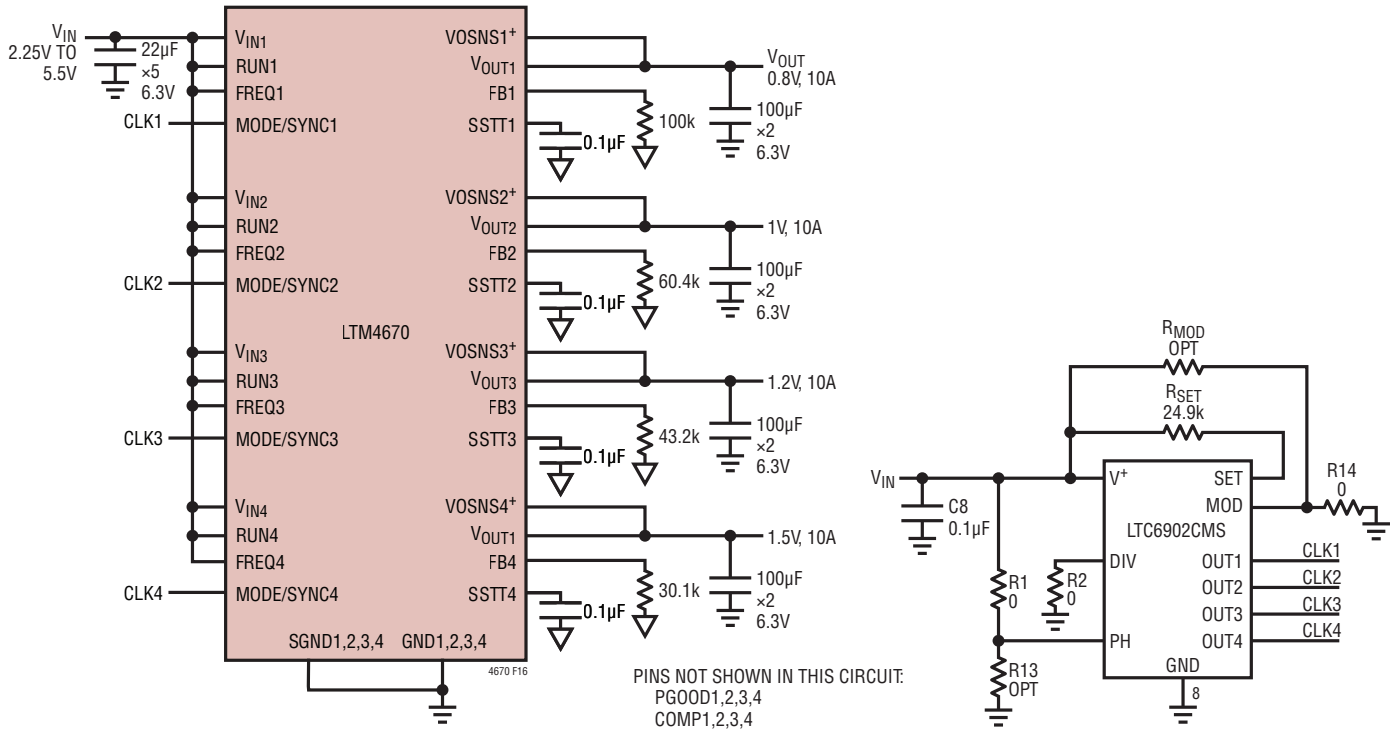


Figure 16. 2MHz High Efficiency, Quad Outputs (Interleaving Operation with External Clock)

TYPICAL APPLICATIONS

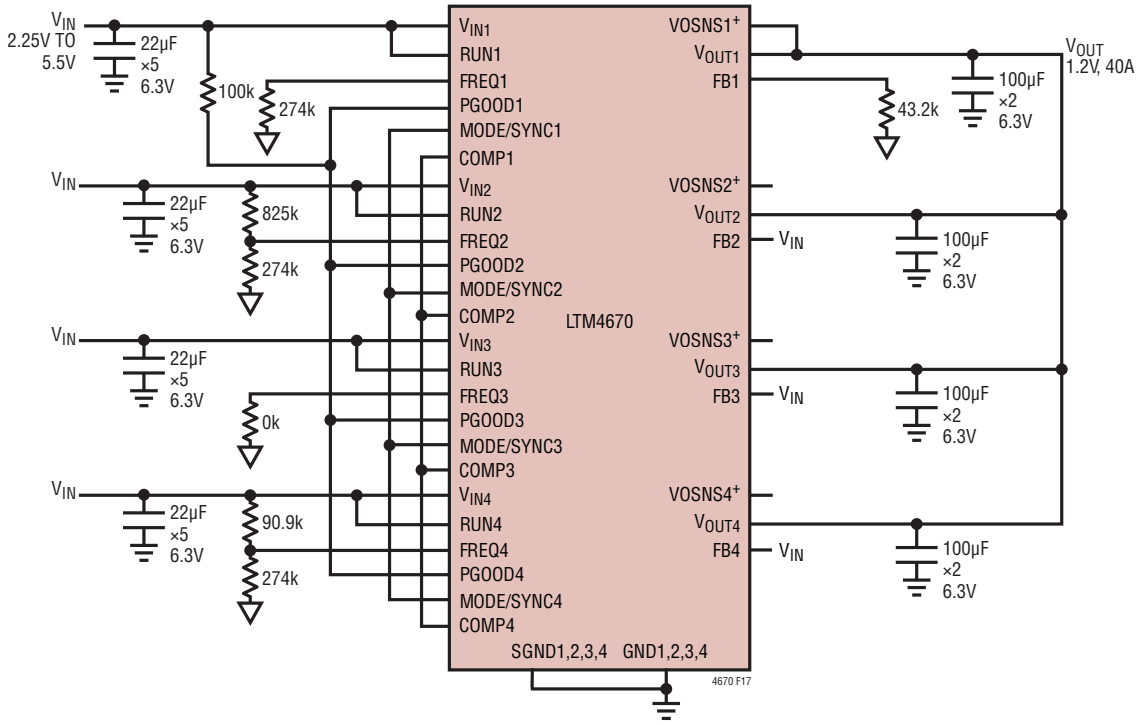


Figure 17. Four-Phase, 2MHz, 1.2V, 40A Design

TYPICAL APPLICATIONS

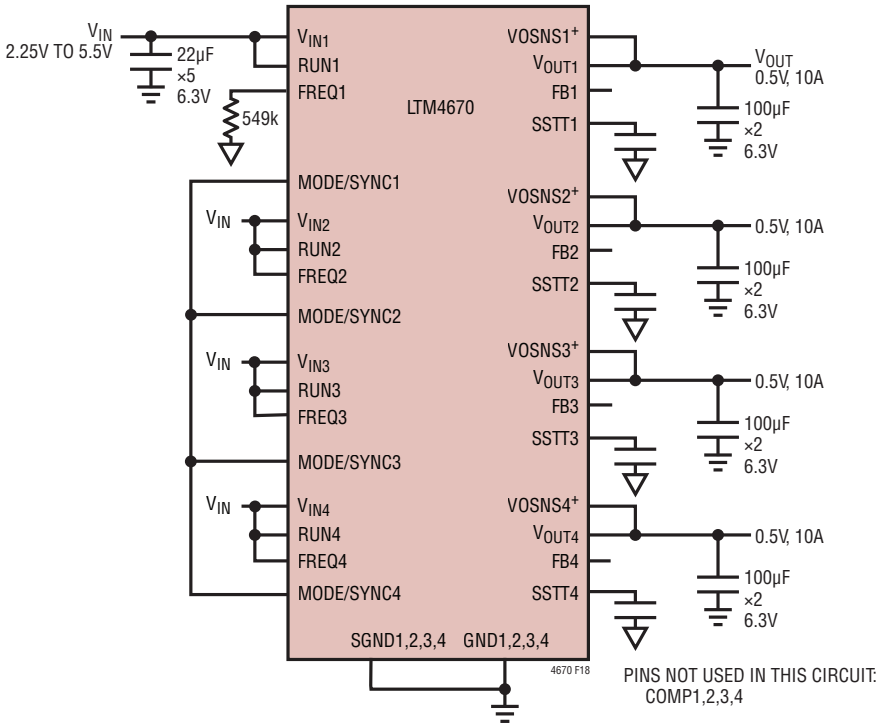


Figure 18. High Efficiency, 1MHz Low Part Count

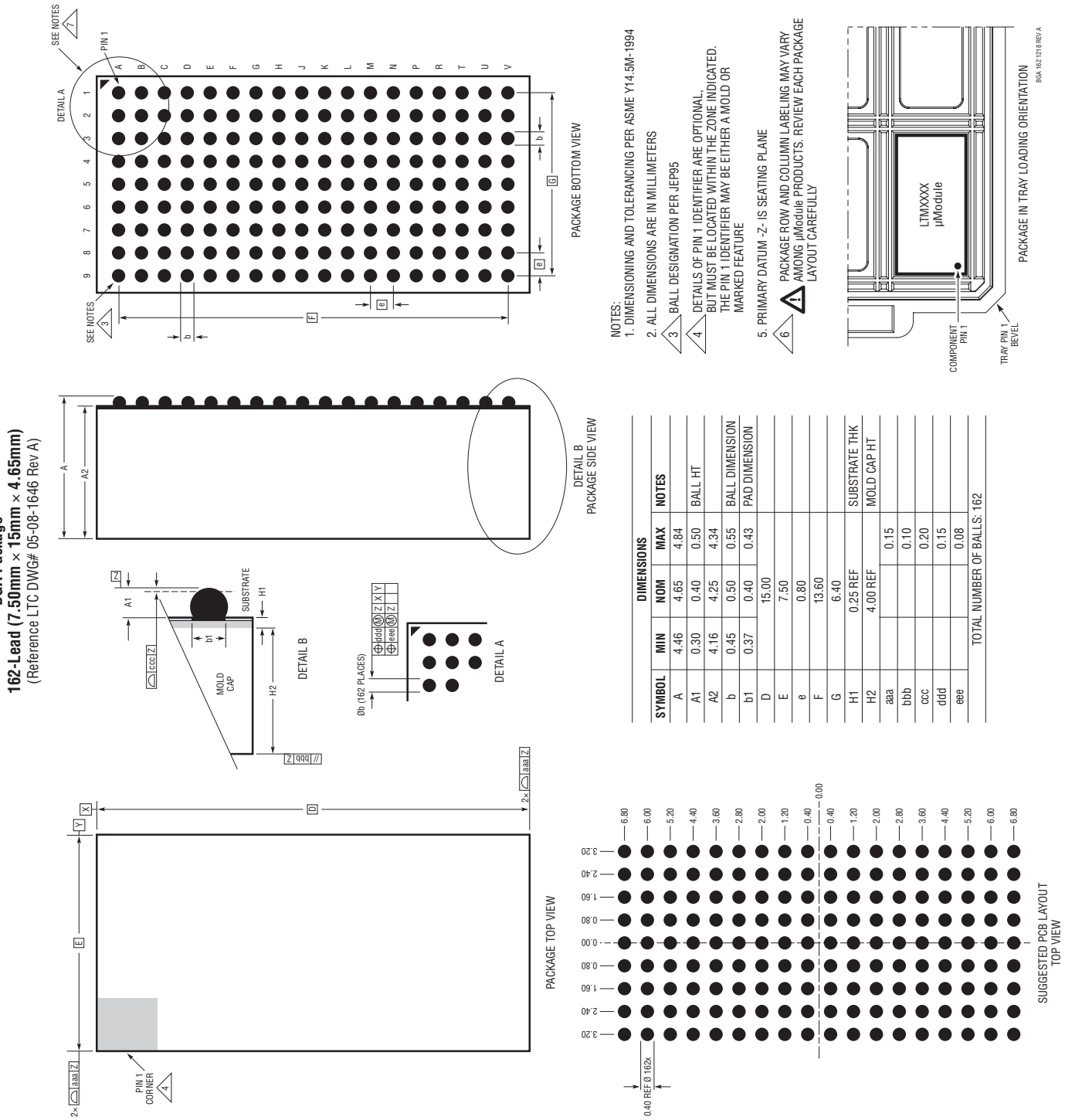
PACKAGE DESCRIPTION

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Table 9. LTM4670 Component BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUT1}	A2	V_{OUT1}	A3	GND1	A4	GND1	A5	GND1	A6	V_{IN1}	A7	GND1	A8	RUN1	A9	VOSNS1+
B1	V_{OUT1}	B2	V_{OUT1}	B3	GND1	B4	SW1	B5	SW1	B6	GND1	B7	V_{IN1}	B8	GND1	B9	FB1
C1	V_{OUT1}	C2	V_{OUT1}	C3	GND1	C4	SW1	C5	SW1	C6	GND1	C7	V_{IN1}	C8	SGND1	C9	COMP1
D1	V_{OUT1}	D2	V_{OUT1}	D3	GND1	D4	GND1	D5	GND1	D6	GND1	D7	V_{IN1}	D8	SSTT1	D9	FREQ1
E1	GND1	E2	GND1	E3	GND1	E4	GND2	E5	GND2	E6	V_{IN2}	E7	MODE/ SYNC1	E8	PGOOD1	E9	VOSNS2+
F1	V_{OUT2}	F2	V_{OUT2}	F3	GND2	F4	GND2	F5	GND2	F6	GND2	F7	V_{IN2}	F8	GND2	F9	FB2
G1	V_{OUT2}	G2	V_{OUT2}	G3	GND2	G4	SW2	G5	SW2	G6	GND2	G7	V_{IN2}	G8	SGND2	G9	COMP2
H1	V_{OUT2}	H2	V_{OUT2}	H3	GND2	H4	SW2	H5	SW2	H6	GND2	H7	V_{IN2}	H8	SSTT2	H9	RUN2
J1	V_{OUT2}	J2	V_{OUT2}	J3	GND2	J4	GND2	J5	GND2	J6	GND2	J7	MODE/ SYNC2	J8	PGOOD2	J9	FREQ2
K1	V_{OUT3}	K2	V_{OUT3}	K3	GND3	K4	GND3	K5	GND3	K6	GND3	K7	GND3	K8	RUN3	K9	VOSNS3+
L1	V_{OUT3}	L2	V_{OUT3}	L3	GND3	L4	SW3	L5	SW3	L6	GND3	L7	V_{IN3}	L8	GND3	L9	FB3
M1	V_{OUT3}	M2	V_{OUT3}	M3	GND3	M4	SW3	M5	SW3	M6	GND3	M7	V_{IN3}	M8	SGND3	M9	COMP3
N1	V_{OUT3}	N2	V_{OUT3}	N3	GND3	N4	GND3	N5	GND3	N6	GND3	N7	V_{IN3}	N8	SSTT3	N9	FREQ3
P1	GND4	P2	GND4	P3	GND4	P4	GND3	P5	GND3	P6	V_{IN3}	P7	MODE/ SYNC3	P8	PGOOD3	P9	VOSNS4+
R1	V_{OUT4}	R2	V_{OUT4}	R3	GND4	R4	GND4	R5	GND4	R6	GND4	R7	V_{IN4}	R8	GND4	R9	FB4
T1	V_{OUT4}	T2	V_{OUT4}	T3	GND4	T4	SW4	T5	SW4	T6	GND4	T7	V_{IN4}	T8	SGND4	T9	COMP4
U1	V_{OUT4}	U2	V_{OUT4}	U3	GND4	U4	SW4	U5	SW4	U6	GND4	U7	V_{IN4}	U8	SSTT4	U9	RUN4
V1	V_{OUT4}	V2	V_{OUT4}	V3	GND4	V4	GND4	V5	GND4	V6	V_{IN4}	V7	MODE/ SYNC4	V8	PGOOD4	V9	FREQ4

PACKAGE DESCRIPTION



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.46	4.65	4.84	
A1	0.30	0.40	0.50	BALL HT
A2	4.16	4.25	4.34	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		15.00		
E		7.50		
e		0.80		
F		13.60		
G		6.40		
H1		0.25 REF		SUBSTRATE THK
H2		4.00 REF		MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 162				

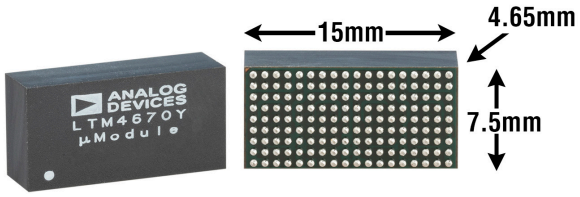
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/22	Changed Lead to Pin in the Pin Configuration drawing.	2
		Changed E3 pin function descritpion from GND2 to GND1.	24
		Added ink marking statement to package photos.	28

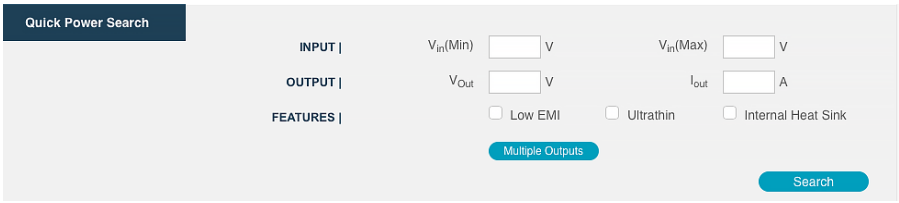
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

PACKAGE PHOTOS

Part marking is either ink mark or laser mark



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4604A	Low V_{IN}, 4A µModule Regulator	$2.375V \le V_{IN} \le 5.5V$, $0.8V \le V_{OUT} \le 5V$, 9mm × 15mm × 2.82mm LGA
LTM4608A	Low V_{IN}, 8A µModule Regulator	$2.7V \le V_{IN} \le 5.5V$, $0.8V \le V_{OUT} \le 5V$, 9mm × 15mm × 2.82mm LGA
LTM4648	Low V_{IN}, 10A µModule Regulator	$2.375V \le V_{IN} \le 5.5V$, $0.8V \le V_{OUT} \le 5V$, 9mm × 15mm × 4.92mm BGA
LTM4658	Low V_{IN}, 10A µModule Regulator	$2.25V \le V_{IN} \le 5.5V$, $0.5V \le V_{OUT} \le V_{IN}$, 4mm × 4mm × 4.32mm LGA
LTM4611	Ultralow V_{IN}, 15A µModule Regulator	$1.5V \le V_{IN} \le 5.5V$, $0.8V \le V_{OUT} \le 5V$, 15mm × 15mm × 4.32mm LGA
LTM4614	Low V_{IN}, Dual 4A µModule Regulator	$2.375V \le V_{IN} \le 5.5V$, $0.8V \le V_{OUT} \le 5V$, 15mm × 15mm × 2.82mm LGA
LTM4615	Low V_{IN}, Triple 4A, 4A, 1.5A, µModule Regulator	$2.375V \le V_{IN} \le 5.5V$, $0.8V \le V_{OUT1}, V_{OUT2} \le 5V$, $0.4V \le V_{OUT3} \le 2.6V$, 15mm × 15mm × 2.82mm LGA
LTM4616	Low V_{IN}, Dual 8A µModule Regulator	$2.7V \le V_{IN} \le 5.5V$, $0.6V \le V_{OUT} \le 5V$, 15mm × 15mm × 2.82mm LGA, 15mm × 15mm × 3.42mm BGA
LTM4648	Low V_{IN}, 10A µModule Regulator	$2.375V \le V_{IN} \le 5.5V$, $0.6V \le V_{OUT} \le 5V$, 9mm × 15mm × 4.92mm BGA
LTM4639	Low V_{IN} with External Bias Voltage, 20A µModule Regulator	$2.375V \le V_{IN} \le 7V$, $0.6V \le V_{OUT} \le 5V$, 15mm × 15mm × 4.92mm BGA
LTM4642	Low V_{IN} with External Bias Voltage, Dual 4A µModule Regulator	$2.375V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5.5V$, 9mm × 11.25mm × 4.92mm BGA
LTM4646	Low V_{IN} with External Bias Voltage, Dual 10A µModule Regulator	$2.375V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5V$, 11.25mm × 15mm × 5.01mm BGA
LTM4662	Low V_{IN} with External Bias Voltage, Dual 15A µModule Regulator	$2.375V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5V$, 11.25mm × 15mm × 5.74mm BGA
LTM4643	Low V_{IN} with External Bias Voltage, Quad 3A µModule Regulator	$2.375V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 3.3V$, 9mm × 15mm × 1.82mm BGA, 9mm × 15mm × 2.42mm BGA
LTM4644	Low V_{IN} with External Bias Voltage, Quad 4A µModule Regulator	$2.375V \le V_{IN} \le 14V$, $0.6V \le V_{OUT} \le 5.5V$, 9mm × 15mm × 5.01mm BGA

© ANALOG DEVICES, INC. 2022