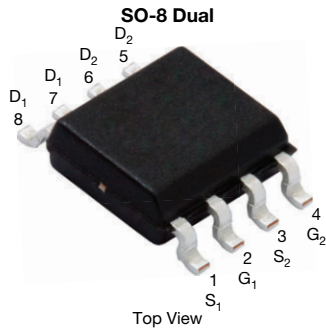


Dual P-Channel 20 V (D-S) MOSFET



FEATURES

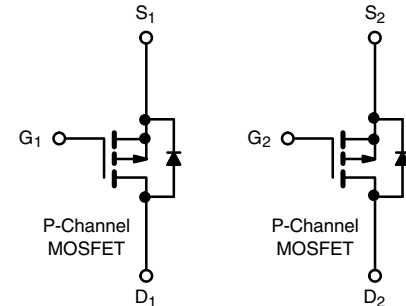
- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Load switch
- DC/DC converter



PRODUCT SUMMARY	
V _{DS} (V)	-20
R _{DS(on)} max. (Ω) at V _{GS} = -4.5 V	0.058
R _{DS(on)} max. (Ω) at V _{GS} = -2.5 V	0.094
Q _g typ. (nC)	8
I _D (A) ^{a, e}	-4
Configuration	Dual

ORDERING INFORMATION	
Package	SO-8
Lead (Pb)-free	Si9933CDY-T1-E3
Lead (Pb)-free and halogen-free	Si9933CDY-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V _{DS}	-20	V	
Gate-source voltage	V _{GS}	± 12		
Continuous drain current (T _J = 150 °C)	I _D	T _C = 25 °C	A	
		T _C = 70 °C		
		T _A = 25 °C		
		T _A = 70 °C		
Pulsed drain current (10 μs pulse width)	I _{DM}	-20	A	
Source-drain current diode current	I _S	T _C = 25 °C		
		T _A = 25 °C		
Single pulse avalanche current	I _{AS}	-6	mJ	
Single-pulse avalanche energy	E _{AS}	1.8		
Maximum power dissipation	P _D	T _C = 25 °C	W	
		T _C = 70 °C		
		T _A = 25 °C		
		T _A = 70 °C		
Operating junction and storage temperature range	T _J , T _{stg}	-50 to +150	°C	

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	LIMIT		UNIT
		TYPICAL	MAXIMUM	
Maximum junction-to-ambient ^{b, d}	R _{thJA}	52	62.5	°C/W
Maximum junction-to-foot (drain)	R _{thJF}	32	40	

Notes

- Based on T_C = 25 °C
- Surface mounted on 1" x 1" FR4 board
- t = 10 s
- Maximum under steady state conditions is 110 °C/W
- Package limited



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.A	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$	-	-19	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	3.1	-	
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.6	-	-1.4	V
Gate-body leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$	-	-	-100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	-	-	-1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	-	-	-10	
On-state drain current ^b	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -10\text{ V}$	-20	-	-	A
Drain-source on-state resistance ^b	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -4.8\text{ A}$	-	0.048	0.058	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -1\text{ A}$	-	0.075	0.094	
Forward transconductance ^b	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -4.8\text{ A}$	-	11	-	S
Dynamic ^a						
Input capacitance	C_{iss}	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	665	-	pF
Output capacitance	C_{oss}		-	140	-	
Reverse transfer capacitance	C_{rss}		-	115	-	
Total gate charge	Q_g	$V_{DS} = -10\text{ V}, V_{GS} = -10\text{ V}, I_D = -4.8\text{ A}$	-	17	26	nC
		$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -4.8\text{ A}$	-	8	12	
Gate-source charge	Q_{gs}		-	2	-	
Gate-drain charge	Q_{gd}		-	3	-	
Gate resistance	R_g	$f = 1\text{ MHz}$	1.2	6	12	Ω
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 2.6\text{ }\Omega$ $I_D \cong -3.8\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$	-	6	12	ns
Rise time	t_r		-	15	23	
Turn-off delay time	$t_{d(off)}$		-	26	39	
Fall time	t_f		-	9	18	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 2.6\text{ }\Omega$ $I_D \cong -3.8\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$	-	21	32	
Rise time	t_r		-	50	75	
Turn-off delay time	$t_{d(off)}$		-	29	44	
Fall time	t_f		-	13	20	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_C = 25\text{ }^\circ\text{C}$	-	-	-2.5	A
Pulse diode forward current ^a	I_{SM}		-	-	-20	
Body diode voltage	V_{SD}	$I_S = -3.8\text{ A}$	-	-0.77	-1.2	V
Body diode reverse recovery time	t_{rr}	$I_F = -3.8\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $T_J = 25\text{ }^\circ\text{C}$	-	30	45	ns
Body diode reverse recovery charge	Q_{rr}		-	17	26	nC
Reverse recovery fall time	t_a		-	16	-	ns
Reverse recovery rise time	t_b		-	14	-	

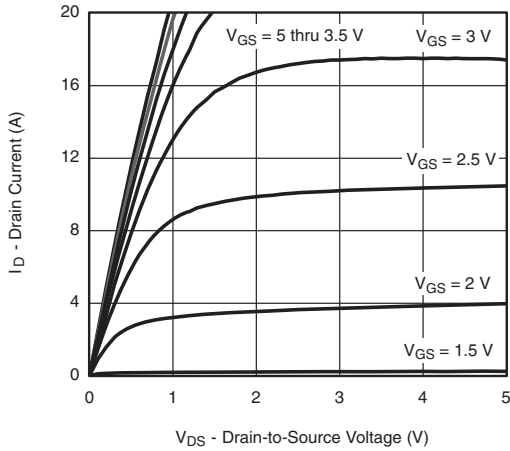
Notes

- a. Guaranteed by design, not subject to production testing
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

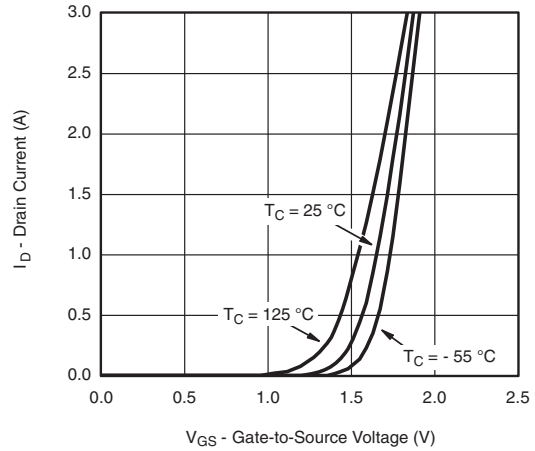
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



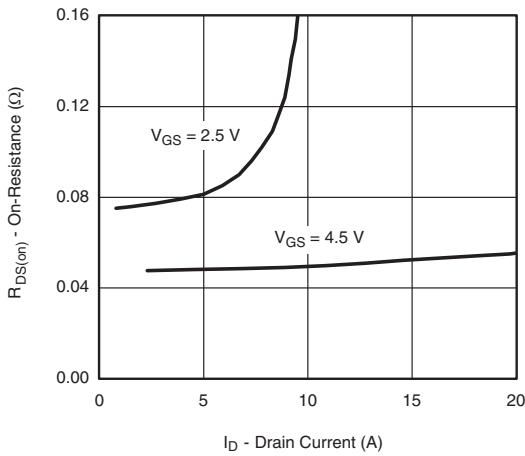
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



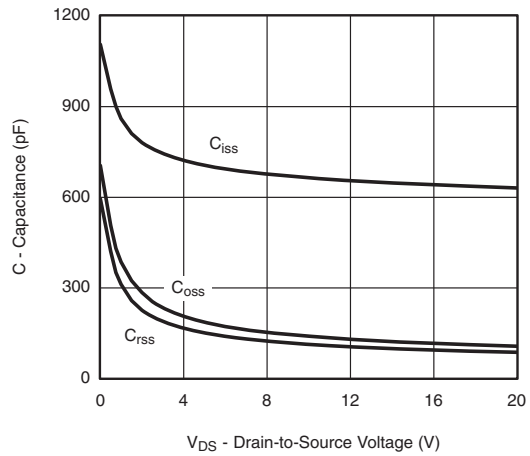
Output Characteristics



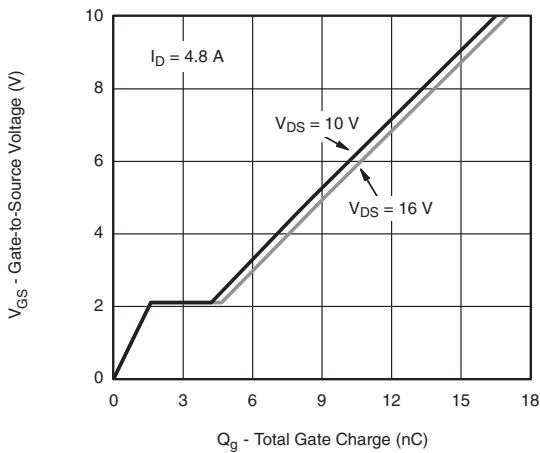
Transfer Characteristics



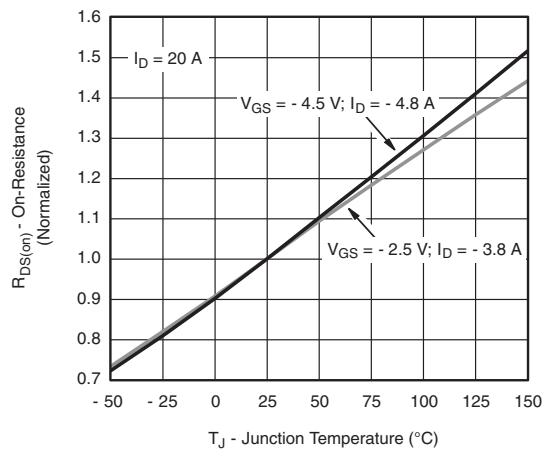
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



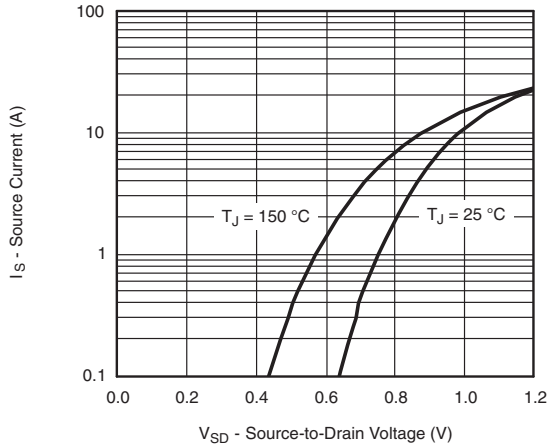
Gate Charge



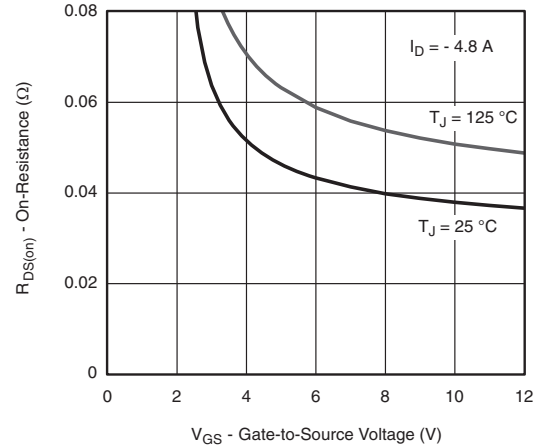
On-Resistance vs. Junction Temperature



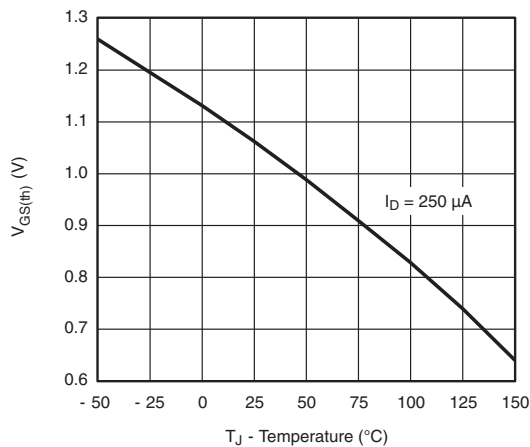
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



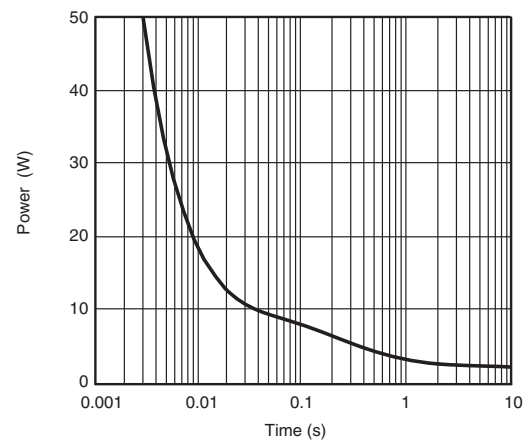
Source-Drain Diode Forward Voltage



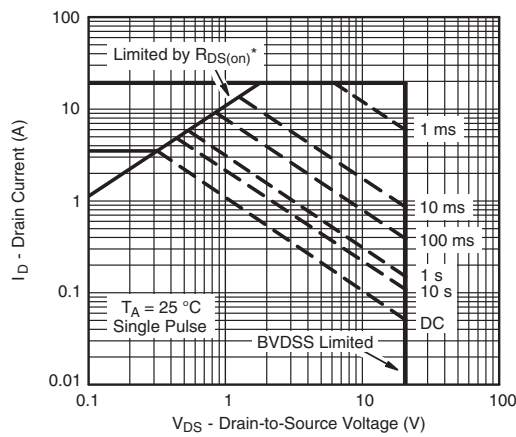
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



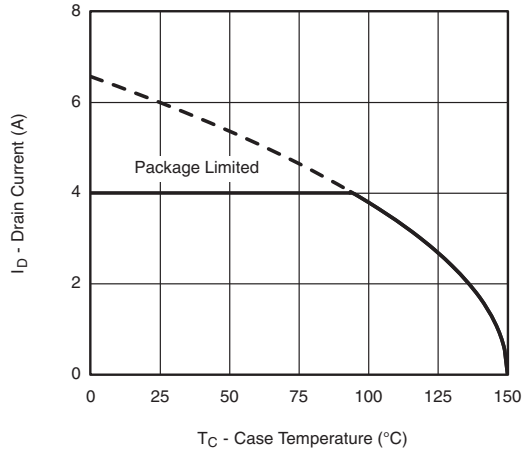
Single Pulse Power, Junction-to-Ambient



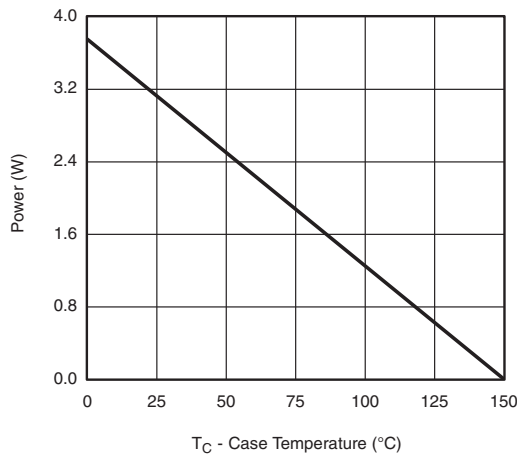
Safe Operating Area, Junction-to-Ambient



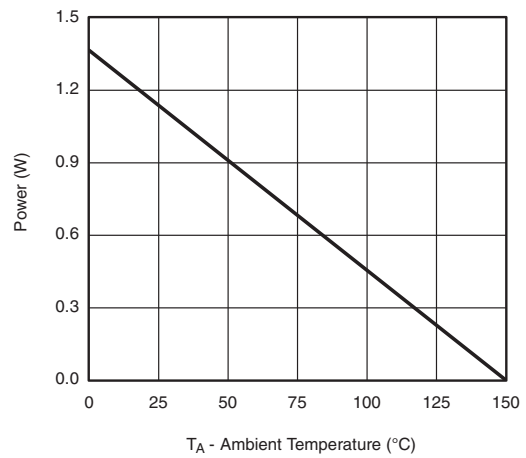
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power Derating, Junction-to-Foot



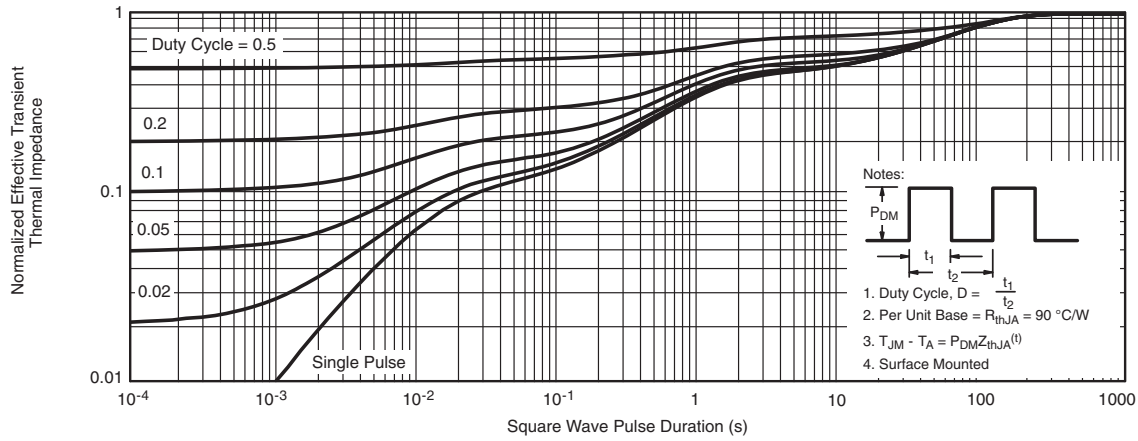
Power Derating, Junction-to-Ambient

Note

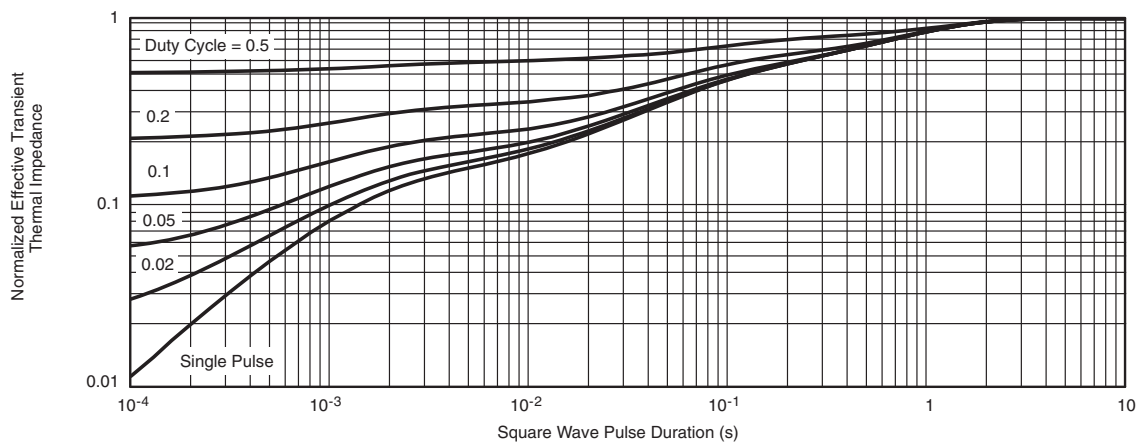
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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