

# MOSFET – P-Channel, POWERTRENCH®

**-30 V, -18 A, 20 mΩ**

## FDMC4435BZ, FDMC4435BZ-F127, FDMC4435BZ-F127-L701

### General Description

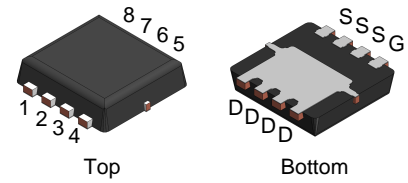
This P-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

### Features

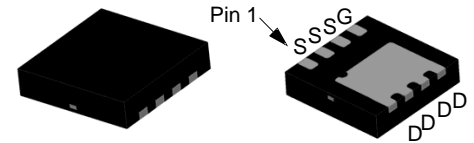
- Max  $r_{DS(on)}$  = 20 mΩ at  $V_{GS} = -10$  V,  $I_D = -8.5$  A
- Max  $r_{DS(on)}$  = 37 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -6.3$  A
- Extended  $V_{GSS}$  Range (-25 V) for Battery Applications
- High Performance Trench Technology for Extremely Low  $r_{DS(on)}$
- High Power and Current Handling Capability
- HBM ESD Protection Level > 7 kV Typical\*
- 100% UIL Tested
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- High Side in DC – DC Buck Converters
- Notebook Battery Power Management
- Load Switch in Notebook

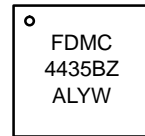
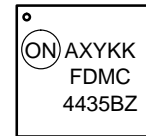


WDFN8 3.3x3.3, 0.65P  
CASE 511DR  
FDMC4435BZ/FDMC4435BZ-F127



WDFN8 3.3x3.3, 0.65P  
CASE 511DQ  
(Option A)  
FDMC4435BZ-F127-L701

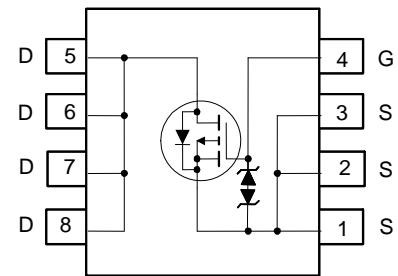
### MARKING DIAGRAM



FDMC4435BZ/ FDMC4435BZ-F127-L701  
FDMC4435BZ-F127

FDMC4435BZ = Specific Device Code  
A = Assembly Location  
XY = 2-Digit Date Code  
KK = 2-Digit Lot Run Traceability Code  
L = Wafer Lot Number  
YW = Assembly Start Week

### PIN ASSIGNMENT



### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

\*The diode connected between the gate and source servers only as protection against ESD. No gate overvoltage rating is implied.

# FDMC4435BZ, FDMC4435BZ-F127, FDMC4435BZ-F127-L701

## MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

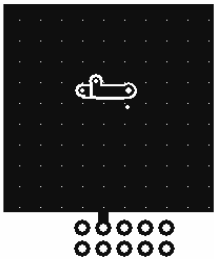
Symbol	Parameter	Rating	Unit	
$V_{DS}$	Drain to Source Voltage	-30	V	
$V_{GS}$	Gate to Source Voltage	$\pm 25$	V	
$I_D$	Drain Current	Continuous	$T_C = 25^\circ\text{C}$	A
		Continuous (Note 1a)	$T_A = 25^\circ\text{C}$	
		Pulsed		
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	32	mJ	
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	31	W
	Power Dissipation (Note 1a)	$T_A = 25^\circ\text{C}$	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to + 150	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $53^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b.  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

2. Starting  $T_J = 25^\circ\text{C}$ ; P-ch:  $L = 1 \text{ mH}$ ,  $I_{AS} = -8 \text{ A}$ ,  $V_{DD} = -27 \text{ V}$ ,  $V_{GS} = -10 \text{ V}$ .

# FDMC4435BZ, FDMC4435BZ-F127, FDMC4435BZ-F127-L701

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = -250 μA, V <sub>GS</sub> = 0 V	-30			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = -250 μA, referenced to 25°C		21		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -24 V, V <sub>GS</sub> = 0 V			-1	μA
		V <sub>DS</sub> = -24 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125°C			-100	
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±25 V, V <sub>DS</sub> = 0 V			±10	μA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250 μA	-1.0	-1.8	-3.0	V
ΔV <sub>GS(th)</sub> / ΔT <sub>J</sub>	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = -250 μA, referenced to 25°C		-5		mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -8.5 A		14	20	mΩ
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -6.3 A		21	37	
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -8.5 A, T <sub>J</sub> = 125°C		20	29	
g <sub>FS</sub>	Forward Transconductance	V <sub>DD</sub> = -5 V, I <sub>D</sub> = -8.5 A		25		S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		1535	2040	pF
C <sub>oss</sub>	Output Capacitance			310	410	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			280	420	pF
R <sub>g</sub>	Gate Resistance	f = 1 MHz		4		Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = -15 V, I <sub>D</sub> = -8.5 A, V <sub>GS</sub> = -10 V, R <sub>GEN</sub> = 6 Ω		10	20	ns
t <sub>r</sub>	Rise Time			9	18	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			35	56	ns
t <sub>f</sub>	Fall Time			19	34	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to -10 V, V <sub>DD</sub> = -15 V, I <sub>D</sub> = -8.5 A		38	53	nC
		V <sub>GS</sub> = 0 V to -4.5 V, V <sub>DD</sub> = -15 V, I <sub>D</sub> = -8.5 A		20	28	nC
Q <sub>gs</sub>	Gate to Source Charge	V <sub>DD</sub> = -15 V, I <sub>D</sub> = -8.5 A		4.3		nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge			11		nC

### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -8.5 A (Note 3)		0.86	1.5	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = -1.9 A (Note 3)		0.74	1.2	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = -8.5 A, di/dt = 100 A/μs		26	40	ns
Q <sub>rr</sub>	Reverse Recovery Charge			12	20	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)

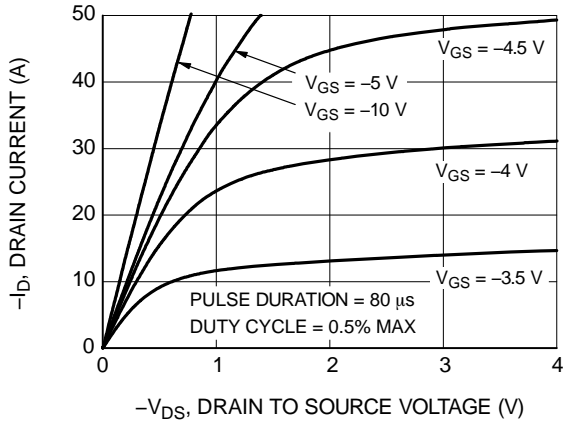


Figure 1. On Region Characteristics

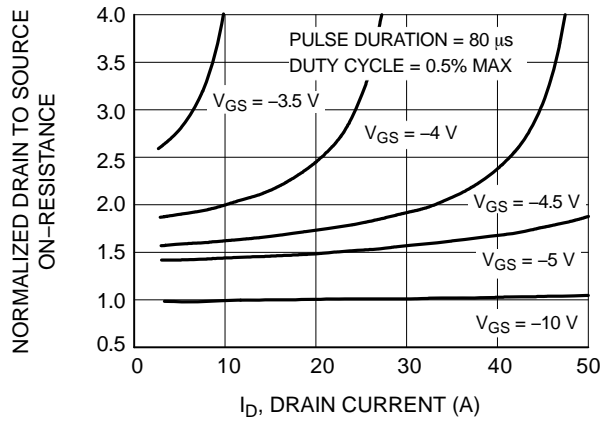


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

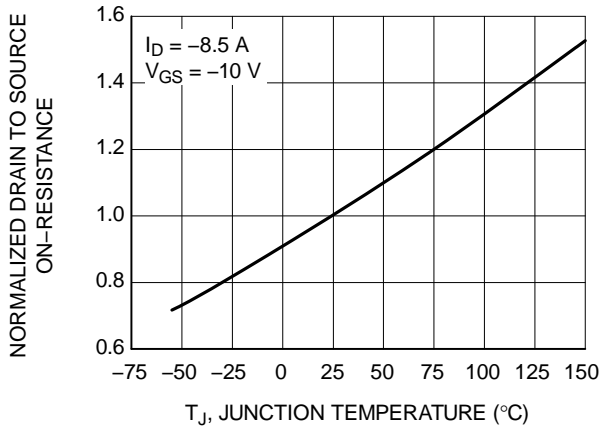


Figure 3. Normalized On Resistance vs. Junction Temperature

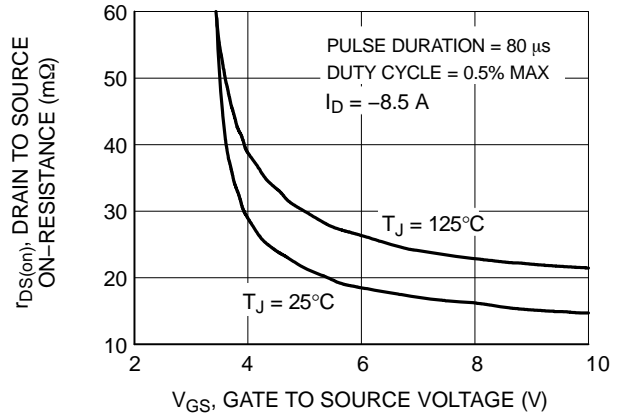


Figure 4. On-Resistance vs. Gate to Source Voltage

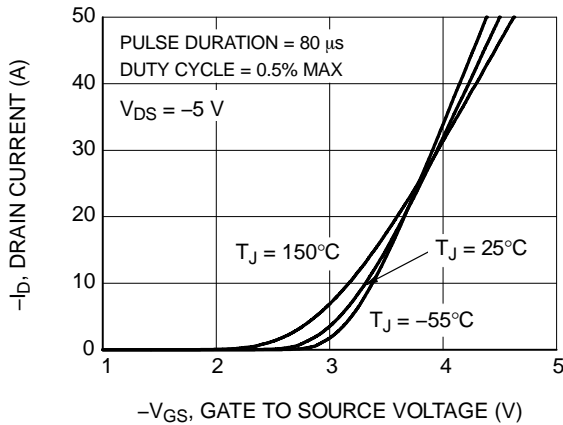


Figure 5. Transfer Characteristics

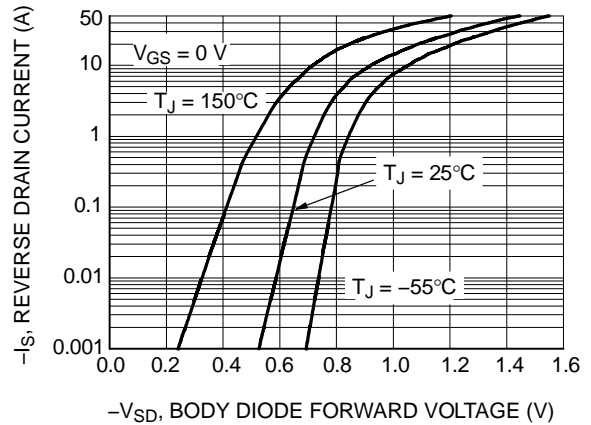


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

# FDMC4435BZ, FDMC4435BZ-F127, FDMC4435BZ-F127-L701

## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED) (CONTINUED)

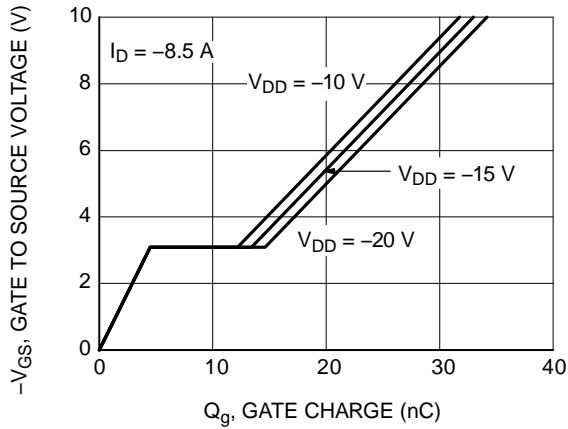


Figure 7. Gate Charge Characteristics

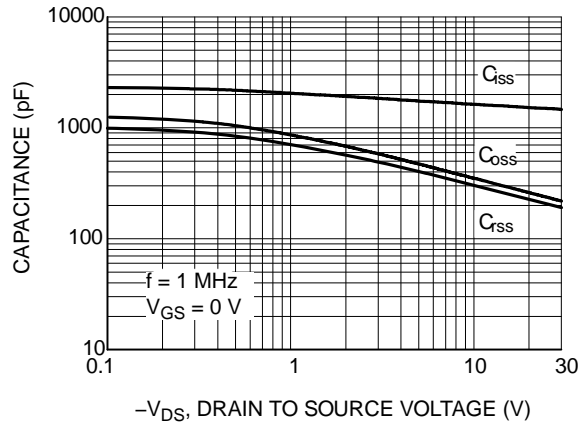


Figure 8. Capacitance vs. Drain to Source Voltage

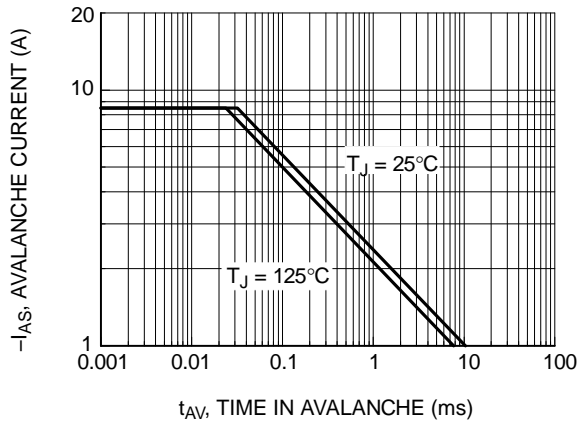


Figure 9. Unclamped Inductive Switching Capability

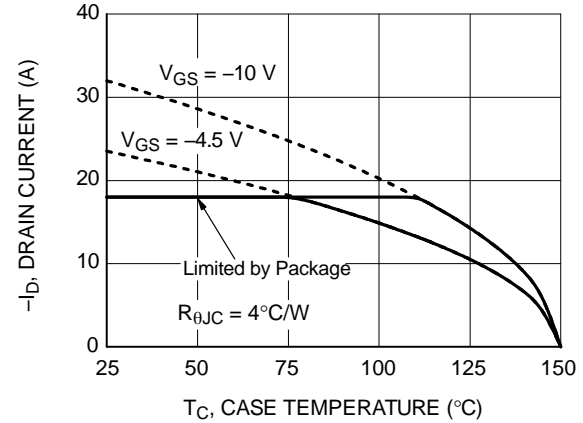


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

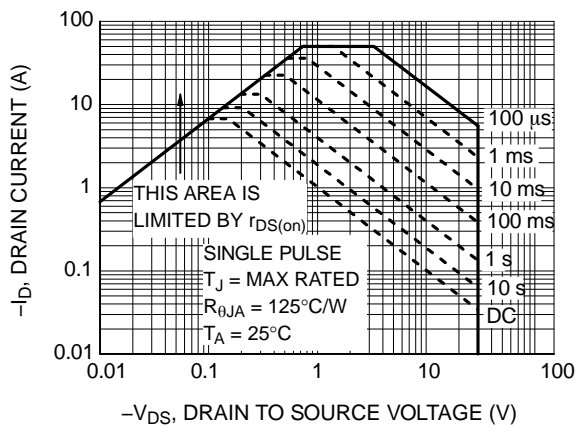


Figure 11. Forward Bias Safe Operating Area

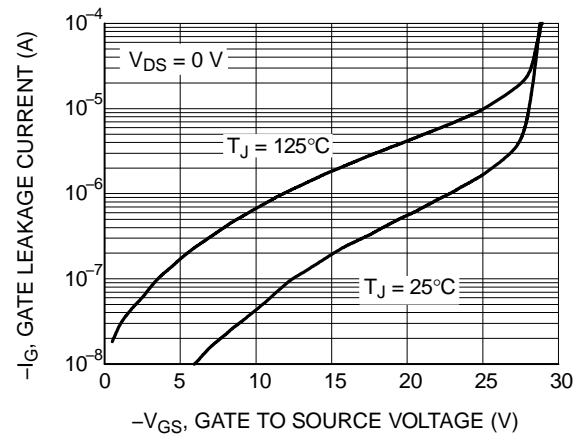


Figure 12.  $I_{GSS}$  vs.  $V_{GSS}$

# FDMC4435BZ, FDMC4435BZ-F127, FDMC4435BZ-F127-L701

## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED) (CONTINUED)

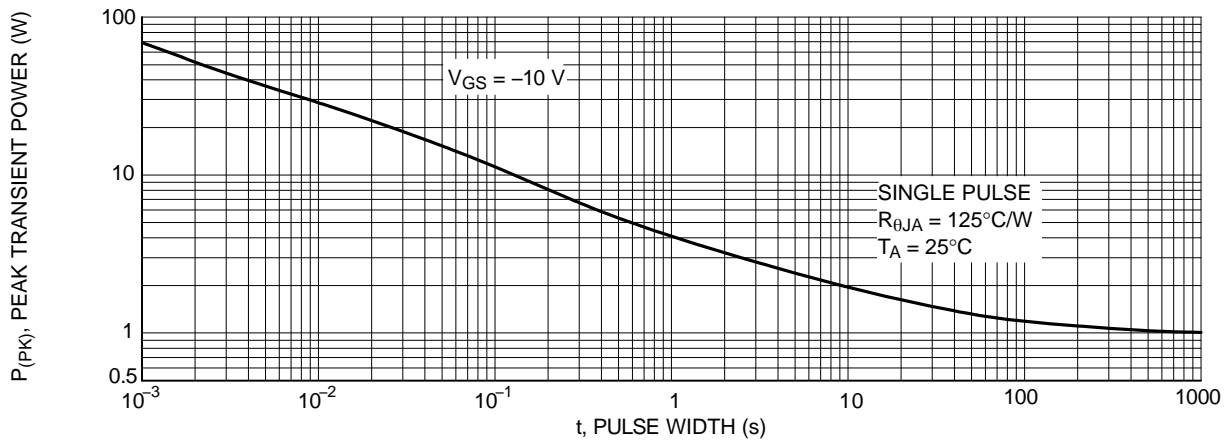


Figure 13. Single Pulse Maximum Power Dissipation

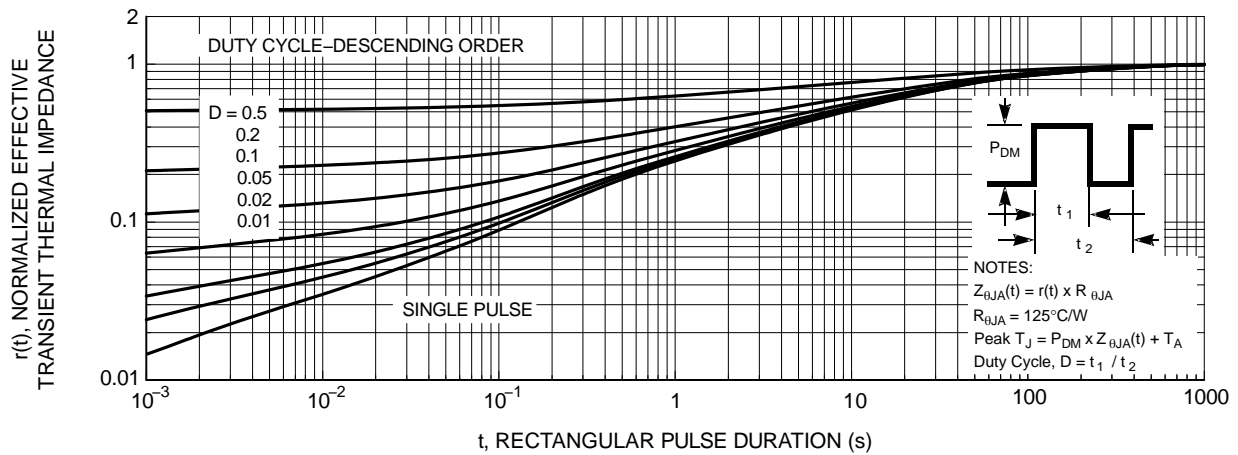


Figure 14. Junction-to-Ambient Transient Thermal Response Curve

### ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping <sup>†</sup>
FDMC4435BZ	FDMC4435BZ	WDFN8 3.3x3.3, 0.65P, case 511DR (Pb-Free)	3000 / Tape & Reel
FDMC4435BZ-F127	FDMC4435BZ	WDFN8 3.3x3.3, 0.65P, case 511DR (Pb-Free)	3000 / Tape & Reel

### DISCONTINUED (Note 4)

FDMC4435BZ-F127-L701	FDMC4435BZ	WDFN8 3.3x3.3, 0.65P, case 511DQ (Pb-Free)	3000 / Tape & Reel
----------------------	------------	--	--------------------

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

4. **DISCONTINUED:** This device is not recommended for new design. Please contact your onsemi representative for information. The most current information on this device may be available on [www.onsemi.com](http://www.onsemi.com).

POWERTRENCH is registered trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

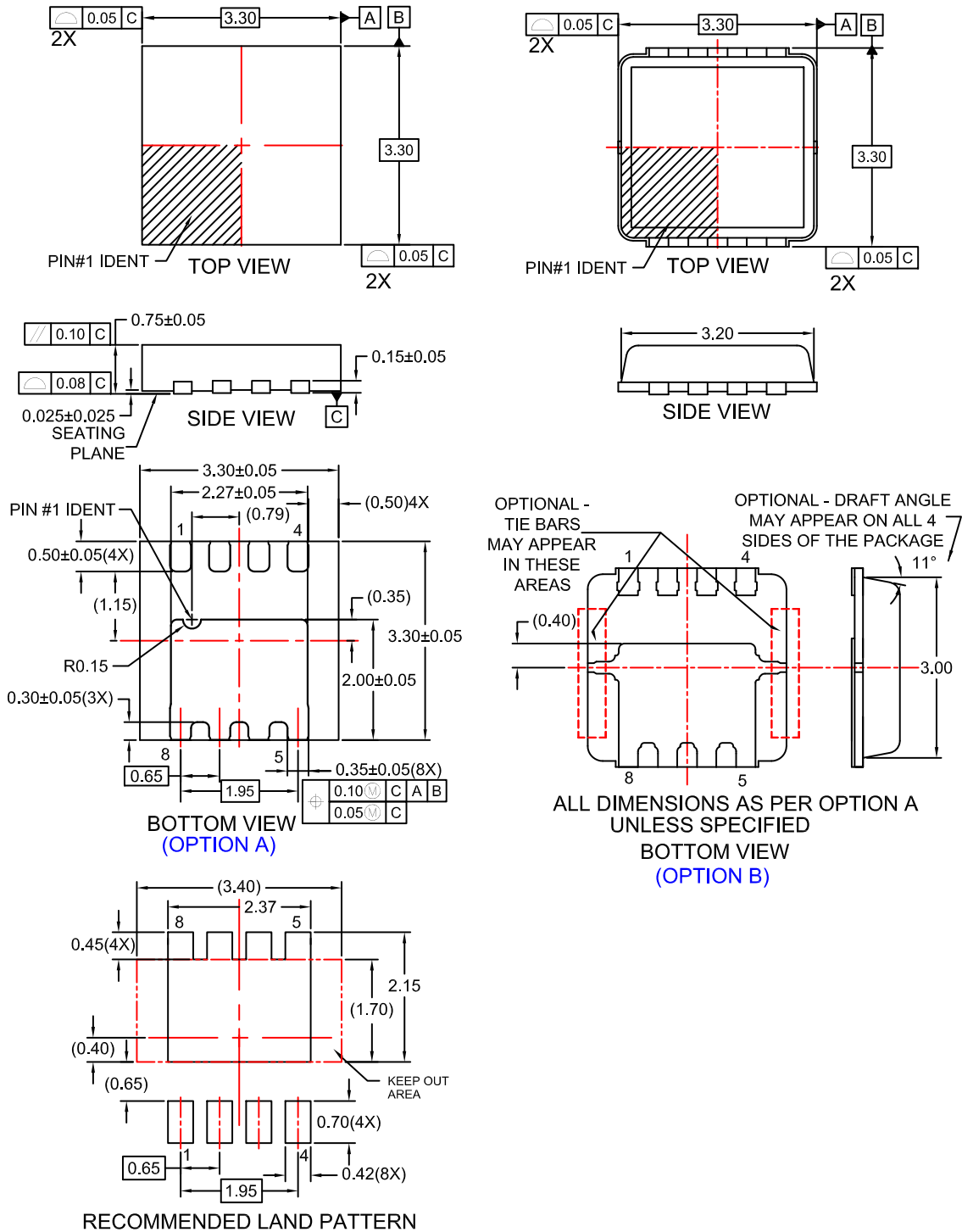
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



## WDFN8 3.3x3.3, 0.65P CASE 511DQ ISSUE O

DATE 31 OCT 2016



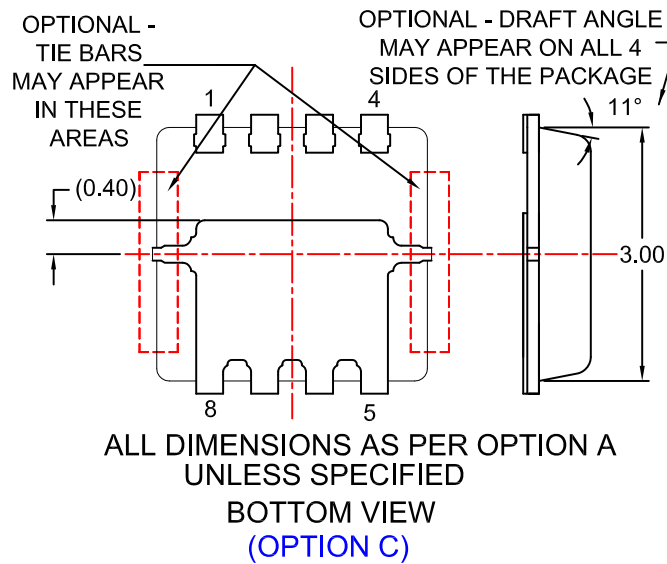
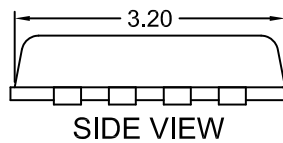
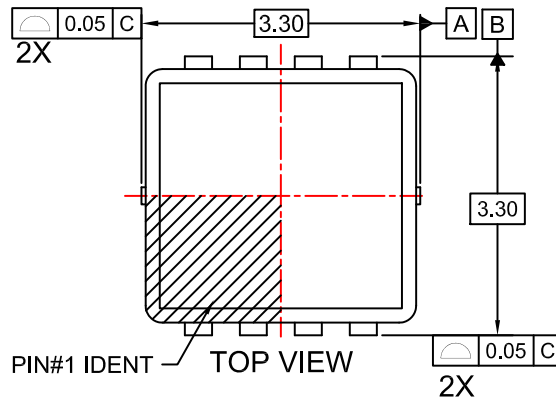
RECOMMENDED LAND PATTERN

<b>DOCUMENT NUMBER:</b>	<b>98AON13648G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>WDFN8 3.3X3.3, 0.65P</b>	<b>PAGE 1 OF 2</b>

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**WDFN8 3.3x3.3, 0.65P**  
CASE 511DQ  
ISSUE O


DATE 31 OCT 2016



**NOTES:**

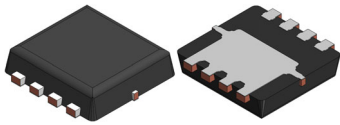
- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
- E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.

<b>DOCUMENT NUMBER:</b>	<b>98AON13648G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>WDFN8 3.3X3.3, 0.65P</b>	<b>PAGE 2 OF 2</b>

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

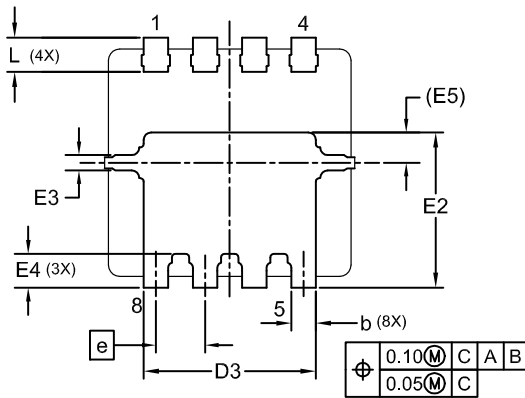
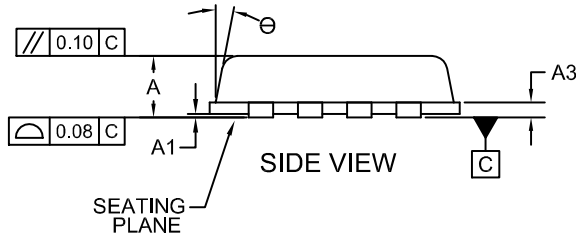
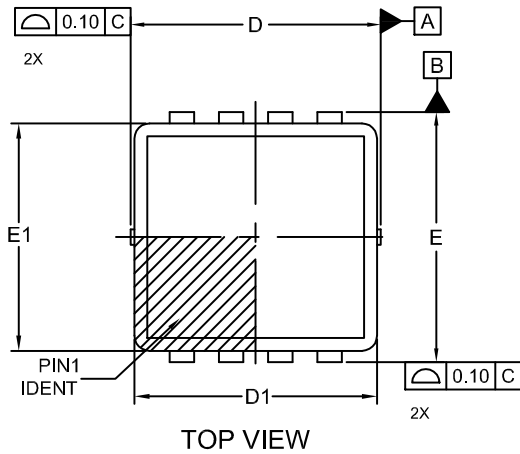


# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**WDFN8 3.3x3.3, 0.65P**  
CASE 511DR  
ISSUE B

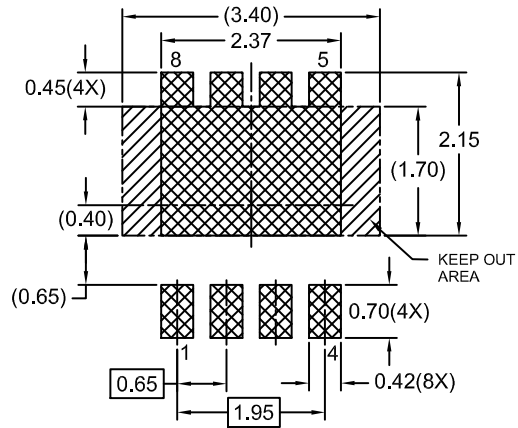
DATE 02 FEB 2022



**NOTES:**

- A. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- B. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
- C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS. MOLD FLASH PROTRUSION OR GATE BURR DOES NOT EXCEED 0.150MM.

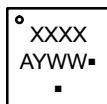
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.15	0.20	0.25
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D1	3.10	3.20	3.30
D3	2.17	2.27	2.37
E	3.20	3.30	3.40
E1	2.90	3.00	3.10
E2	1.95	2.05	2.15
E3	0.15	0.20	0.25
E4	0.30	0.40	0.50
E5	0.40 REF		
e	0.65 BSC		
L	0.30	0.40	0.50
θ	0°	-	12°



**RECOMMENDED LAND PATTERN**

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

**GENERIC MARKING DIAGRAM\***



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

(Note: Microdot may be in either location)

<b>DOCUMENT NUMBER:</b>	<b>98AON13650G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>WDFN8 3.3x3.3, 0.65P</b>	<b>PAGE 1 OF 1</b>

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)