74LVC1G125

Bus buffer/line driver; 3-state

Rev. 17 — 11 July 2024 | Product data sheet

1. General description

The 74LVC1G125 is a single buffer/line driver with 3-state output. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power consumption
- I_{OFF} circuitry provides partial Power-down mode operation
- ±24 mA output drive (V_{CC} = 3.0 V)
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

nexperia

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G125GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74LVC1G125GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74LVC1G125GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74LVC1G125GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	SOT1115
74LVC1G125GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202
74LVC1G125GX	-40 °C to +125 °C	X2SON5	plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 × 0.8 × 0.32 mm	SOT1226-3
74LVC1G125GZ	-40 °C to +125 °C	XSON5	plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm	SOT8065-1

4. Marking

Table 2. Marking

Type number	Marking code[1]
74LVC1G125GW	VM
74LVC1G125GV	V25
74LVC1G125GM	VM
74LVC1G125GN	VM
74LVC1G125GS	VM
74LVC1G125GX	VM
74LVC1G125GZ	VM

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

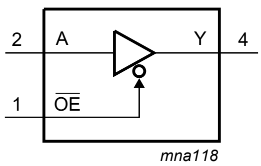


Fig. 1. Logic symbol

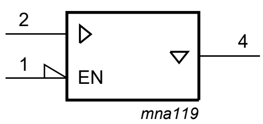


Fig. 2. IEC logic symbol

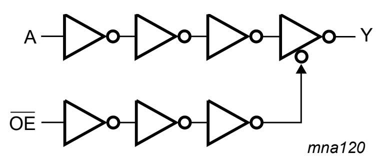
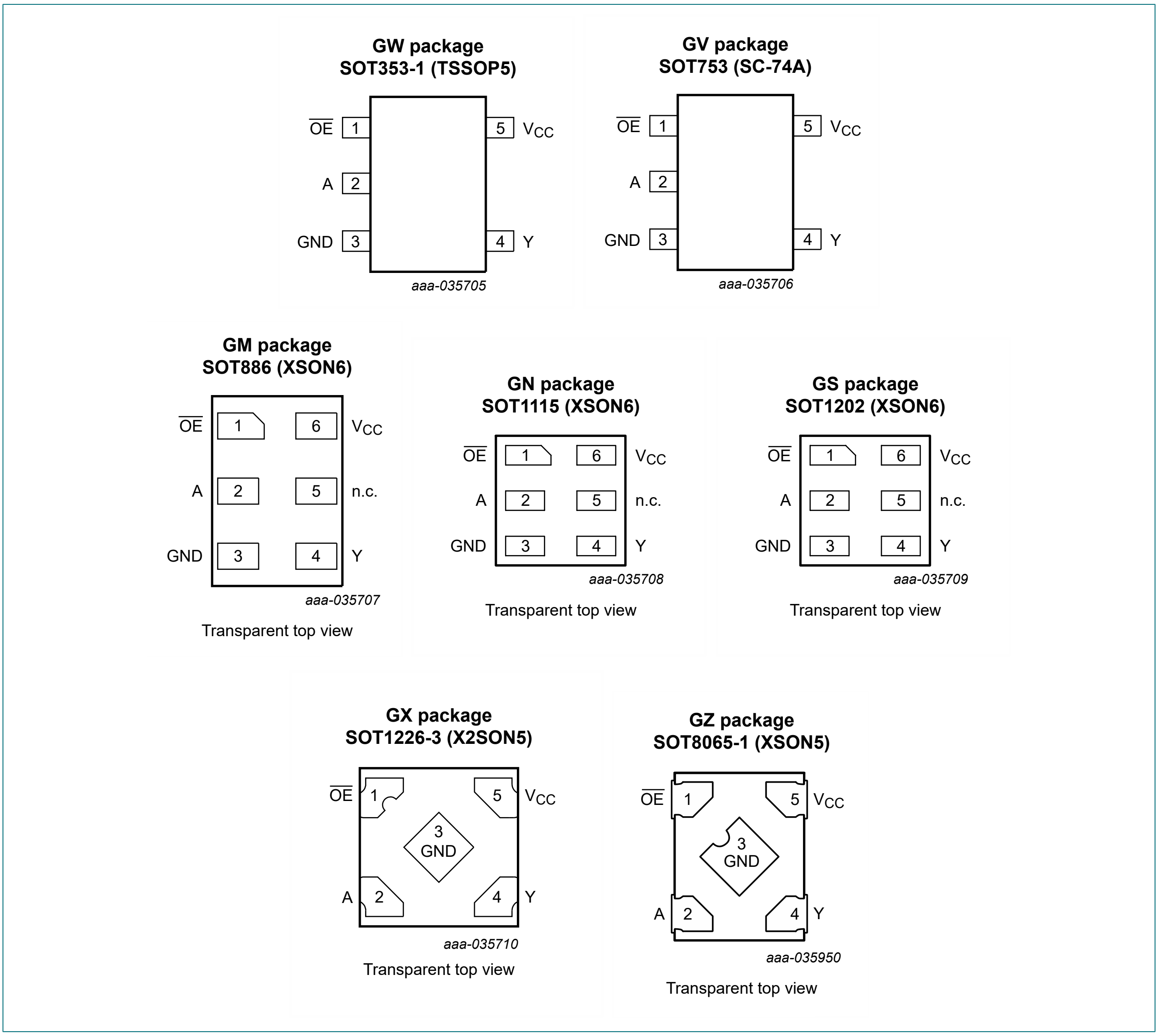


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP5, SC-74A, X2SON5 and XSON5	XSON6	
$\overline{OE}$	1	1	output enable input
A	2	2	data input
GND	3	3	ground (0 V)
Y	4	4	data output
n.c.	-	5	not connected
V_{CC}	5	6	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Output
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage	[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
V_O	output voltage	Active mode [1]	-0.5	V_{CC} + 0.5	V
		Power-down mode; V_{CC} = 0 V [1]	-0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [2]	-	250	mW
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT753 (SC-74A) package: P_{tot} derates linearly with 3.8 mW/K above 85 °C.
For SOT886 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT1115 (XSON6) package: P_{tot} derates linearly with 3.2 mW/K above 71 °C.
For SOT1202 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT1226-3 (X2SON5) package: P_{tot} derates linearly with 3.0 mW/K above 67 °C.
For SOT8065-1 (XSON5) package: P_{tot} derates linearly with 3.2 mW/K above 72 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	-	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	-	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 1.65 V to 5.5 V; I_O = 100 μA	-	-	0.1	V
		V_{CC} = 1.65 V; I_O = 4 mA	-	-	0.45	V
		V_{CC} = 2.3 V; I_O = 8 mA	-	-	0.3	V
		V_{CC} = 2.7 V; I_O = 12 mA	-	-	0.4	V
		V_{CC} = 3.0 V; I_O = 24 mA	-	-	0.55	V
		V_{CC} = 4.5 V; I_O = 32 mA	-	-	0.55	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 1.65 V to 5.5 V; I_O = -100 μA	V_{CC} - 0.1	-	-	V
		V_{CC} = 1.65 V; I_O = -4 mA	1.2	-	-	V
		V_{CC} = 2.3 V; I_O = -8 mA	1.9	-	-	V
		V_{CC} = 2.7 V; I_O = -12 mA	2.2	-	-	V
		V_{CC} = 3.0 V; I_O = -24 mA	2.3	-	-	V
		V_{CC} = 4.5 V; I_O = -32 mA	3.8	-	-	V

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
I_I	input leakage current	V_{CC} = 0 V to 5.5 V; V_I = 5.5 V or GND	-	±0.1	±1	μA
I_{OZ}	OFF-state output current	V_{CC} = 3.6 V; V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND	-	±0.1	±2	μA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	±0.1	±2	μA
I_{CC}	supply current	V_I = 5.5 V or GND; V_{CC} = 1.65 V to 5.5 V; I_O = 0 A	-	0.1	4	μA
ΔI_{CC}	additional supply current	per pin; V_{CC} = 2.3 V to 5.5 V; V_I = V_{CC} - 0.6 V; I_O = 0 A	-	5	500	μA
C_I	input capacitance		-	5	-	pF
T_{amb} = -40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 1.65 V to 5.5 V; I_O = 100 μA	-	-	0.1	V
		V_{CC} = 1.65 V; I_O = 4 mA	-	-	0.70	V
		V_{CC} = 2.3 V; I_O = 8 mA	-	-	0.45	V
		V_{CC} = 2.7 V; I_O = 12 mA	-	-	0.60	V
		V_{CC} = 3.0 V; I_O = 24 mA	-	-	0.80	V
		V_{CC} = 4.5 V; I_O = 32 mA	-	-	0.80	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 1.65 V to 5.5 V; I_O = -100 μA	V_{CC} - 0.1	-	-	V
		V_{CC} = 1.65 V; I_O = -4 mA	0.95	-	-	V
		V_{CC} = 2.3 V; I_O = -8 mA	1.7	-	-	V
		V_{CC} = 2.7 V; I_O = -12 mA	1.9	-	-	V
		V_{CC} = 3.0 V; I_O = -24 mA	2.0	-	-	V
		V_{CC} = 4.5 V; I_O = -32 mA	3.4	-	-	V
I_I	input leakage current	V_{CC} = 0 V to 5.5 V; V_I = 5.5 V or GND	-	-	±1	μA
I_{OZ}	OFF-state output current	V_{CC} = 3.6 V; V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND	-	-	±2	μA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	-	±2	μA
I_{CC}	supply current	V_I = 5.5 V or GND; V_{CC} = 1.65 V to 5.5 V; I_O = 0 A	-	-	4	μA
ΔI_{CC}	additional supply current	per pin; V_{CC} = 2.3 V to 5.5 V; V_I = V_{CC} - 0.6 V; I_O = 0 A	-	-	500	μA

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 6.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	A to Y; see Fig. 4 [2]						
		V_{CC} = 1.65 V to 1.95 V	1.0	3.3	8.0	1.0	10.5	ns
		V_{CC} = 2.3 V to 2.7 V	0.5	2.2	5.5	0.5	7	ns
		V_{CC} = 2.7 V	0.5	2.5	5.5	0.5	7	ns
		V_{CC} = 3.0 V to 3.6 V	0.5	2.1	4.5	0.5	6	ns
		V_{CC} = 4.5 V to 5.5 V	0.5	1.7	4.0	0.5	5.5	ns
t_{en}	enable time	$\overline{OE}$ to Y; see Fig. 5 [3]						
		V_{CC} = 1.65 V to 1.95 V	1.0	4.1	9.4	1.0	12	ns
		V_{CC} = 2.3 V to 2.7 V	0.5	2.8	6.6	0.5	8.5	ns
		V_{CC} = 2.7 V	0.5	3.3	6.6	0.5	8.5	ns
		V_{CC} = 3.0 V to 3.6 V	0.5	2.4	5.3	0.5	7	ns
		V_{CC} = 4.5 V to 5.5 V	0.5	2.1	5.0	0.5	6.5	ns
t_{dis}	disable time	$\overline{OE}$ to Y; see Fig. 5 [4]						
		V_{CC} = 1.65 V to 1.95 V	1.0	4.3	9.2	1.0	12	ns
		V_{CC} = 2.3 V to 2.7 V	0.5	2.7	5.0	0.5	6.5	ns
		V_{CC} = 2.7 V	0.5	3.0	5.0	0.5	6.5	ns
		V_{CC} = 3.0 V to 3.6 V	0.5	3.1	5.0	0.5	6.5	ns
		V_{CC} = 4.5 V to 5.5 V	0.5	2.2	4.2	0.5	5.5	ns
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC} [5]						
		output enabled	-	25	-	-	-	pF
		output disabled	-	6	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] t_{en} is the same as t_{PZH} and t_{PZL}.
[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

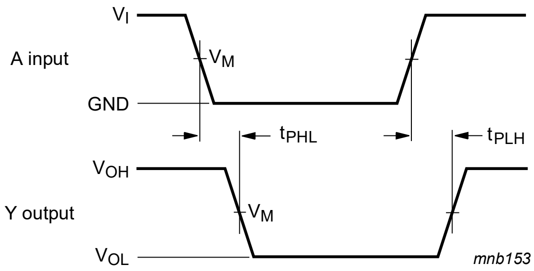
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

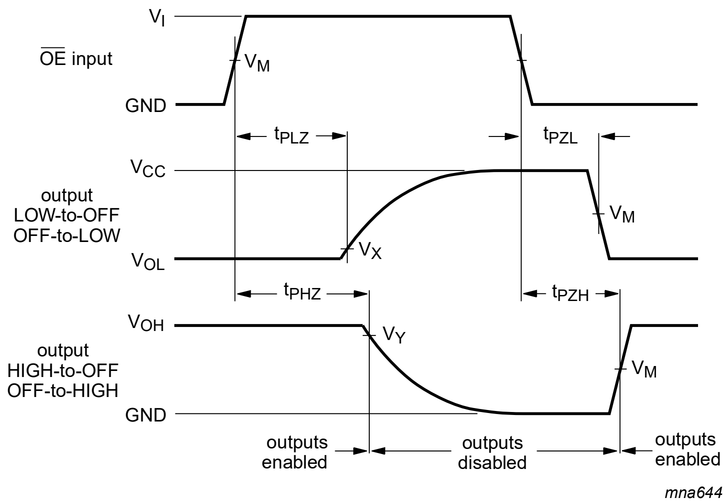
11.1. Waveforms and test circuit



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. Input A to output Y propagation delay times



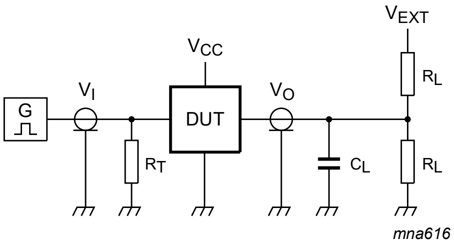
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. 3-state enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.3 V to 2.7 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
4.5 V to 5.5 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 10.
Definitions for test circuit:
R_L = Load resistance;
C_L = Load capacitance including jig and probe capacitance;
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator;
V_{EXT} = External voltage for measuring switching times.

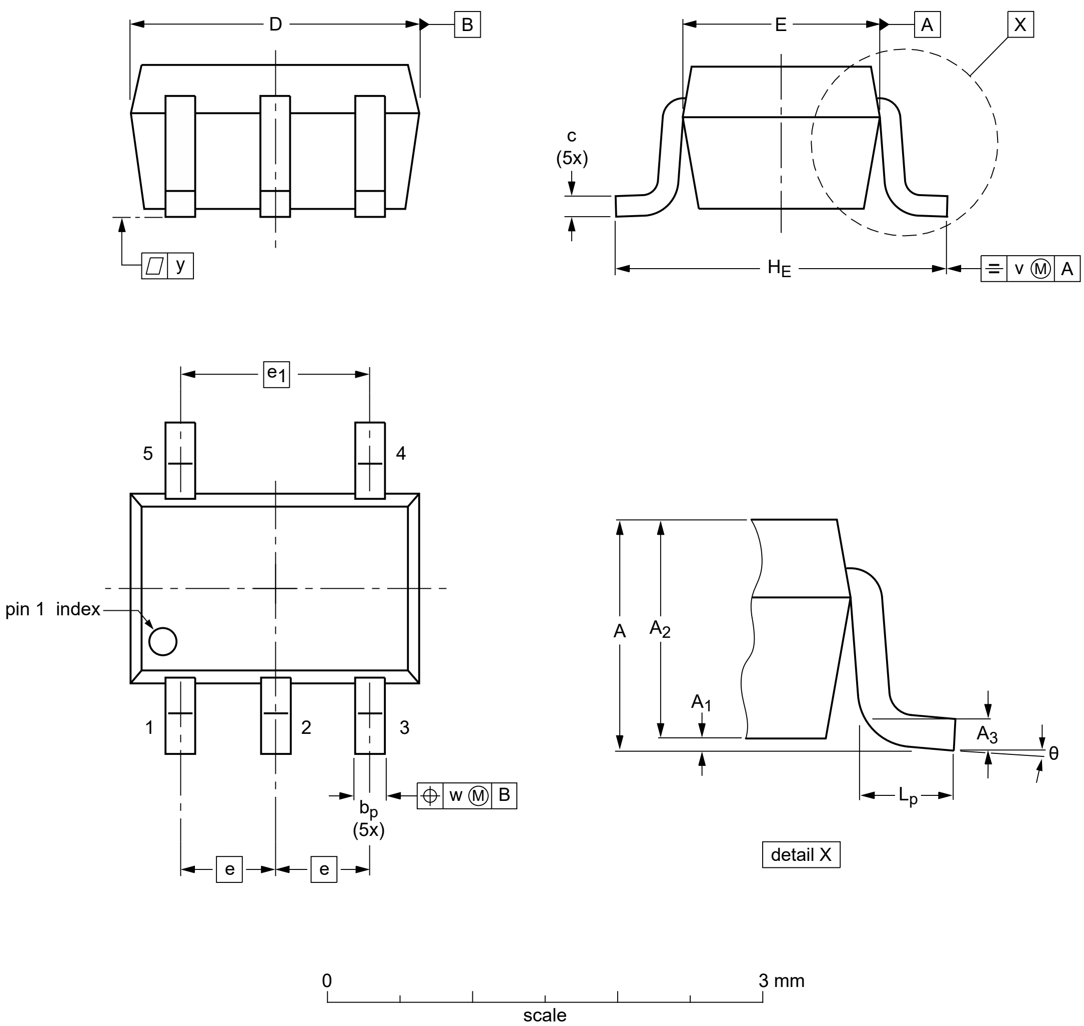
Fig. 6. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open	GND	2 × V_{CC}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	2 × V_{CC}
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	2 × V_{CC}

12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm **SOT353-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	e_1	H_E	L_p	v	w	y	θ
mm	max	1.1	0.1	1.0	0.15	0.30	0.25	2.2	1.35	0.65	1.3	2.4	0.46	0.3	0.1	0.1	8°
	min	0.8	0	0.8		0.15	0.08	1.8	1.15			1.8	0.26				0°

Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot353-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT353-1		MO-203	SC-88A			~~21-12-15~~ 21-12-16

Fig. 7. Package outline SOT353-1 (TSSOP5)

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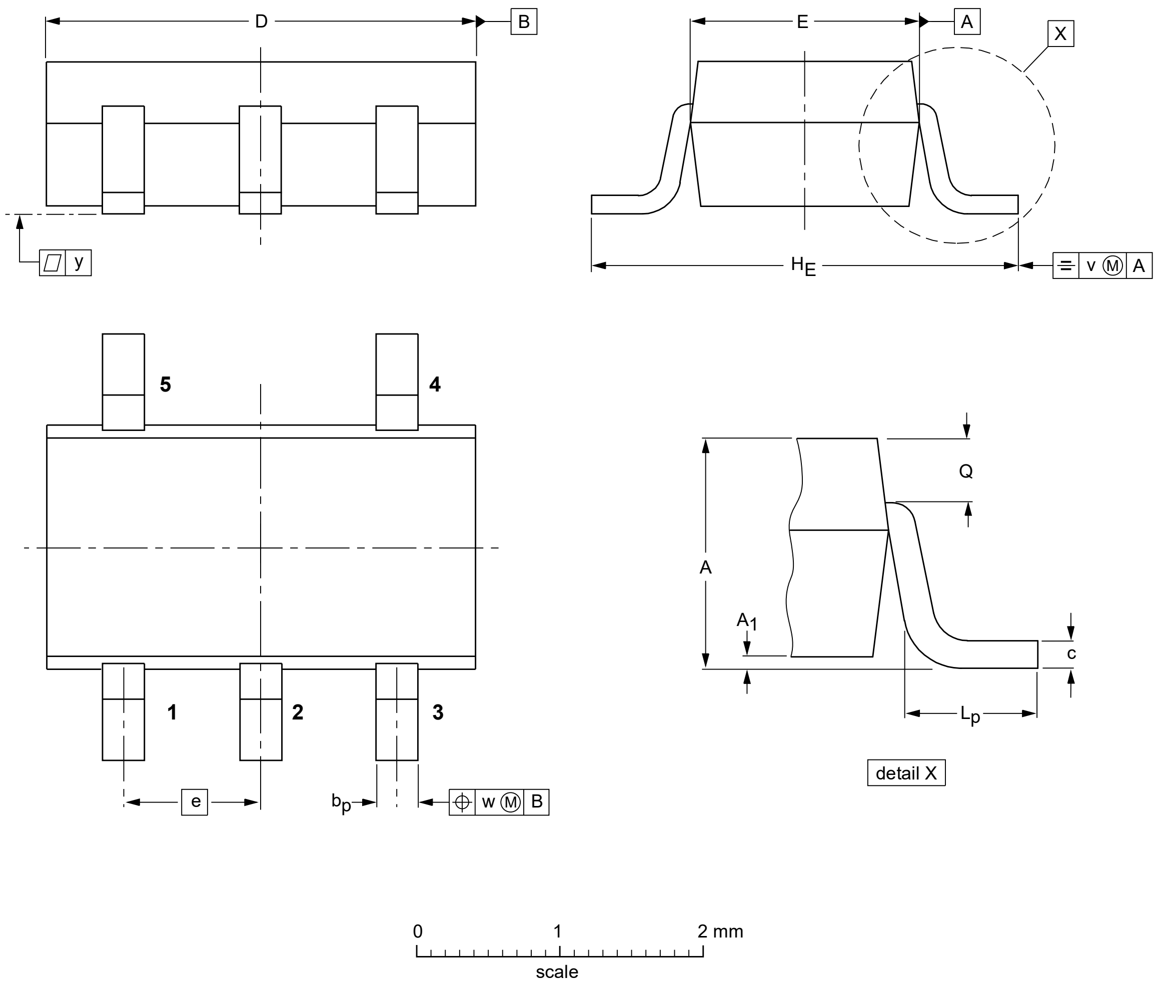
Plastic surface-mounted package; 5 leads **SOT753**



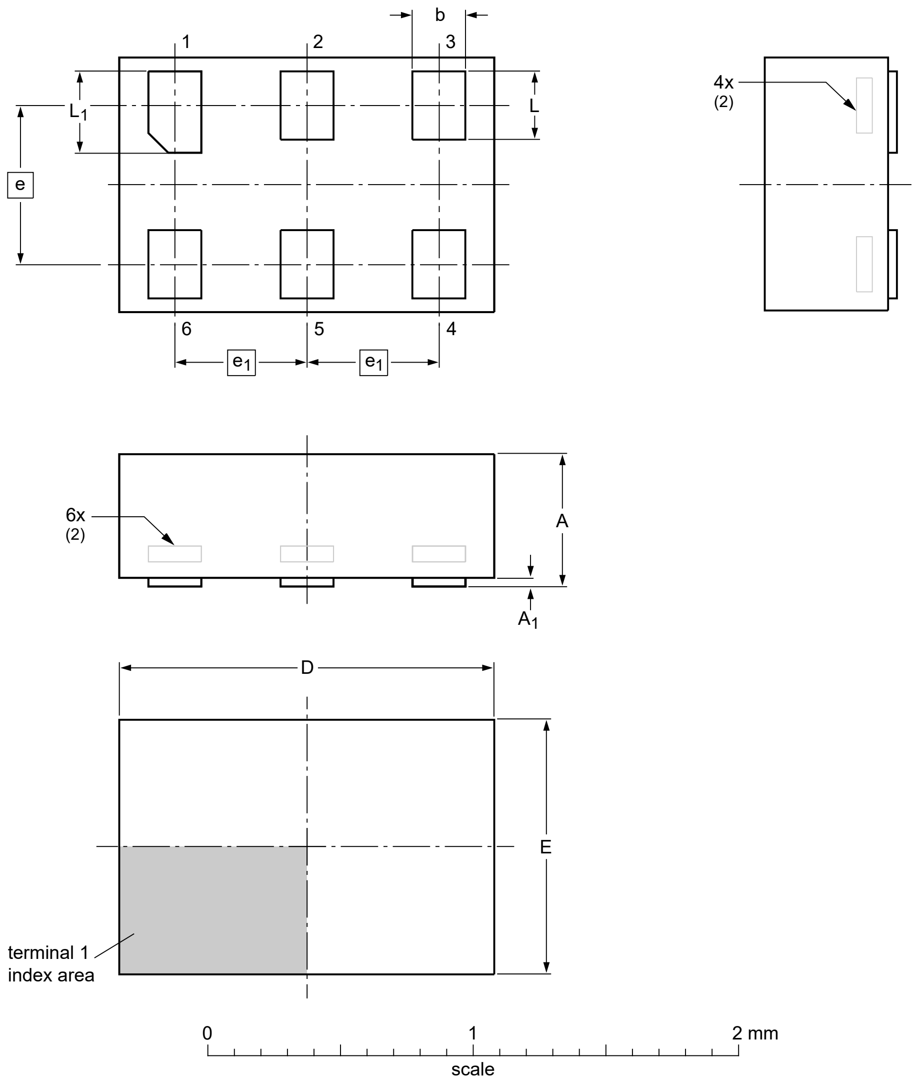
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			~~02-04-16~~ 06-03-16

Fig. 8. Package outline SOT753 (SC-74A)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm — SOT886



Dimensions (mm are the original dimensions)

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
	max	0.5	0.04	0.25	1.50	1.05			0.35	0.40
mm	nom			0.20	1.45	1.00	0.6	0.5	0.30	0.35
	min			0.17	1.40	0.95			0.27	0.32

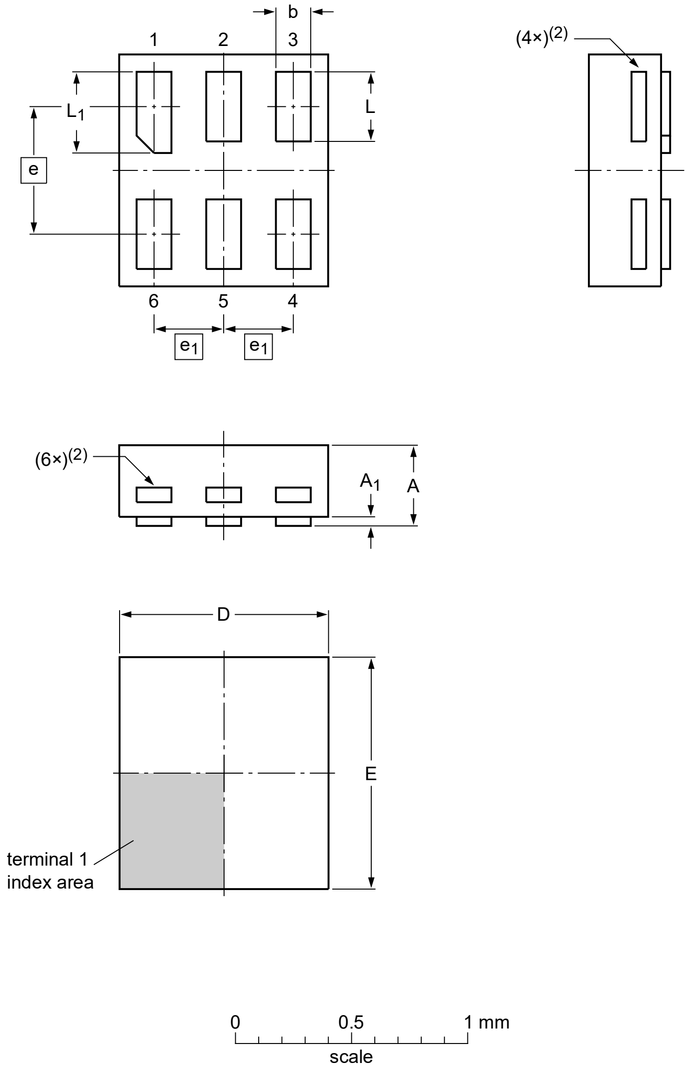
Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

sot886_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-22~~ 12-01-05

Fig. 9. Package outline SOT886 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm **SOT1115**



Dimensions

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
	max	0.35	0.04	0.20	0.95	1.05			0.35	0.40
mm	nom			0.15	0.90	1.00	0.55	0.3	0.30	0.35
	min			0.12	0.85	0.95			0.27	0.32

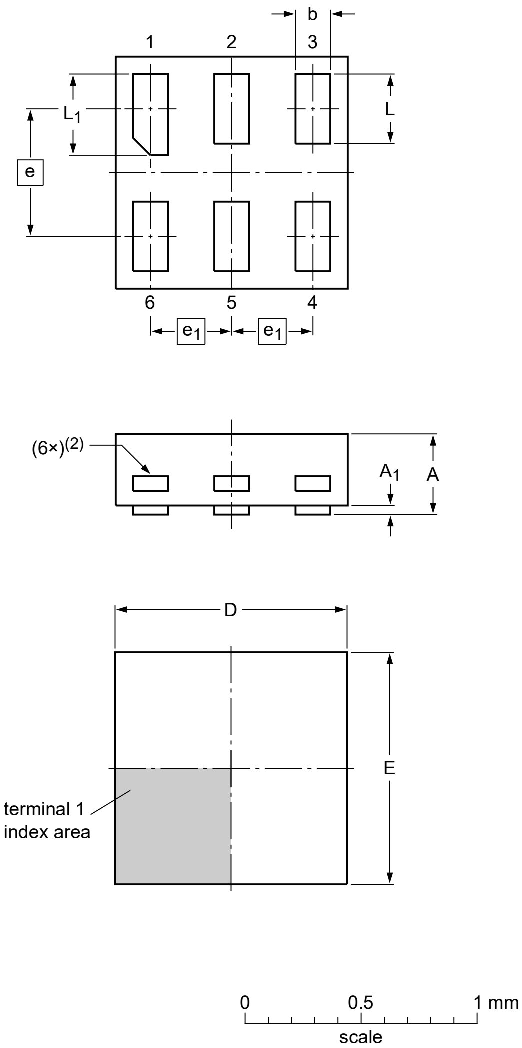
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1115_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1115						~~10-04-02~~ 10-04-07

Fig. 10. Package outline SOT1115 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm **SOT1202**



Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
	max	0.35	0.04	0.20	1.05	1.05			0.35	0.40
mm	nom			0.15	1.00	1.00	0.55	0.35	0.30	0.35
	min			0.12	0.95	0.95			0.27	0.32

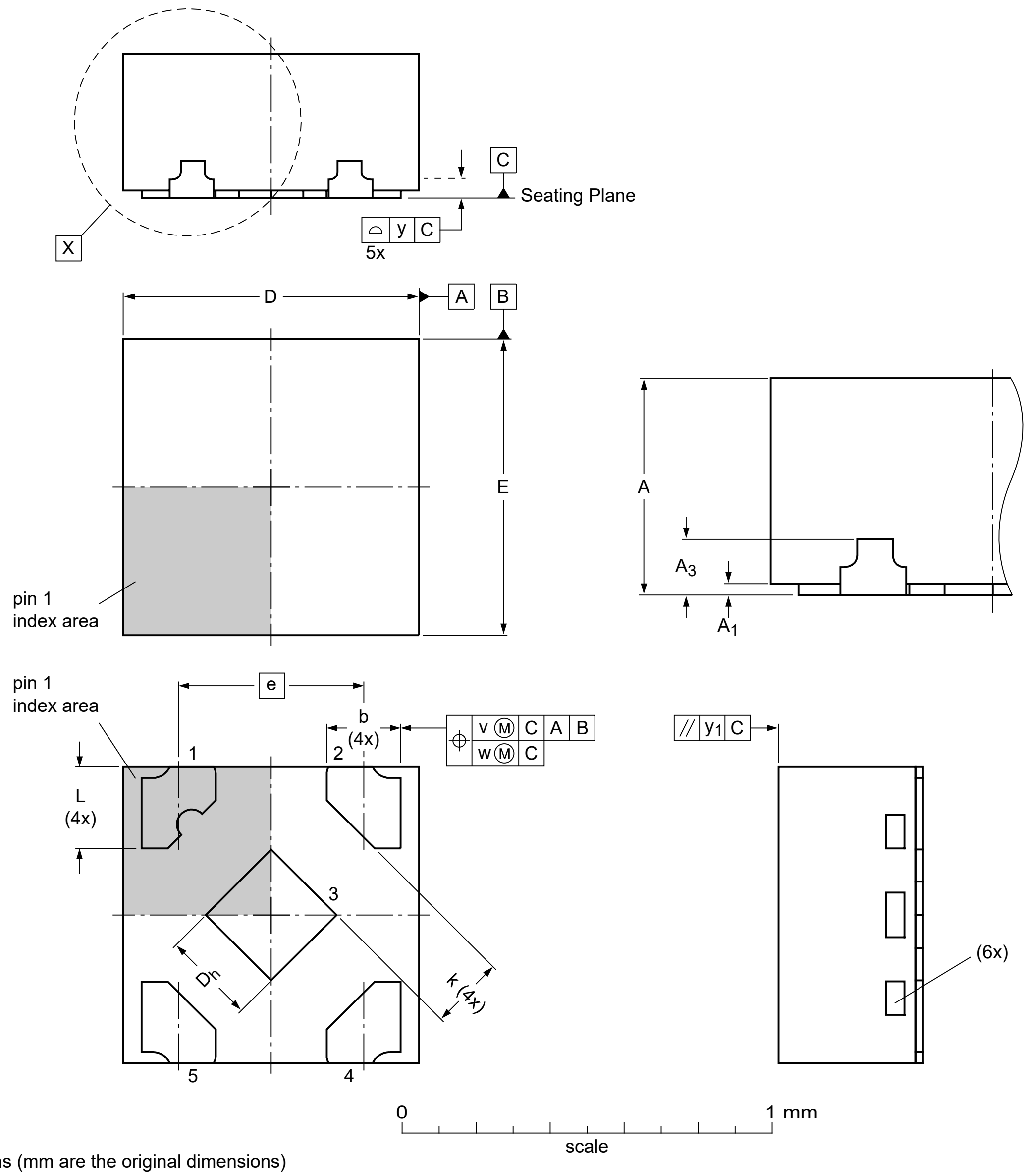
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1202_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1202						~~10-04-02~~ 10-04-06

Fig. 11. Package outline SOT1202 (XSON6)

X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 x 0.8 x 0.32 mm **SOT1226-3**



Dimensions (mm are the original dimensions)

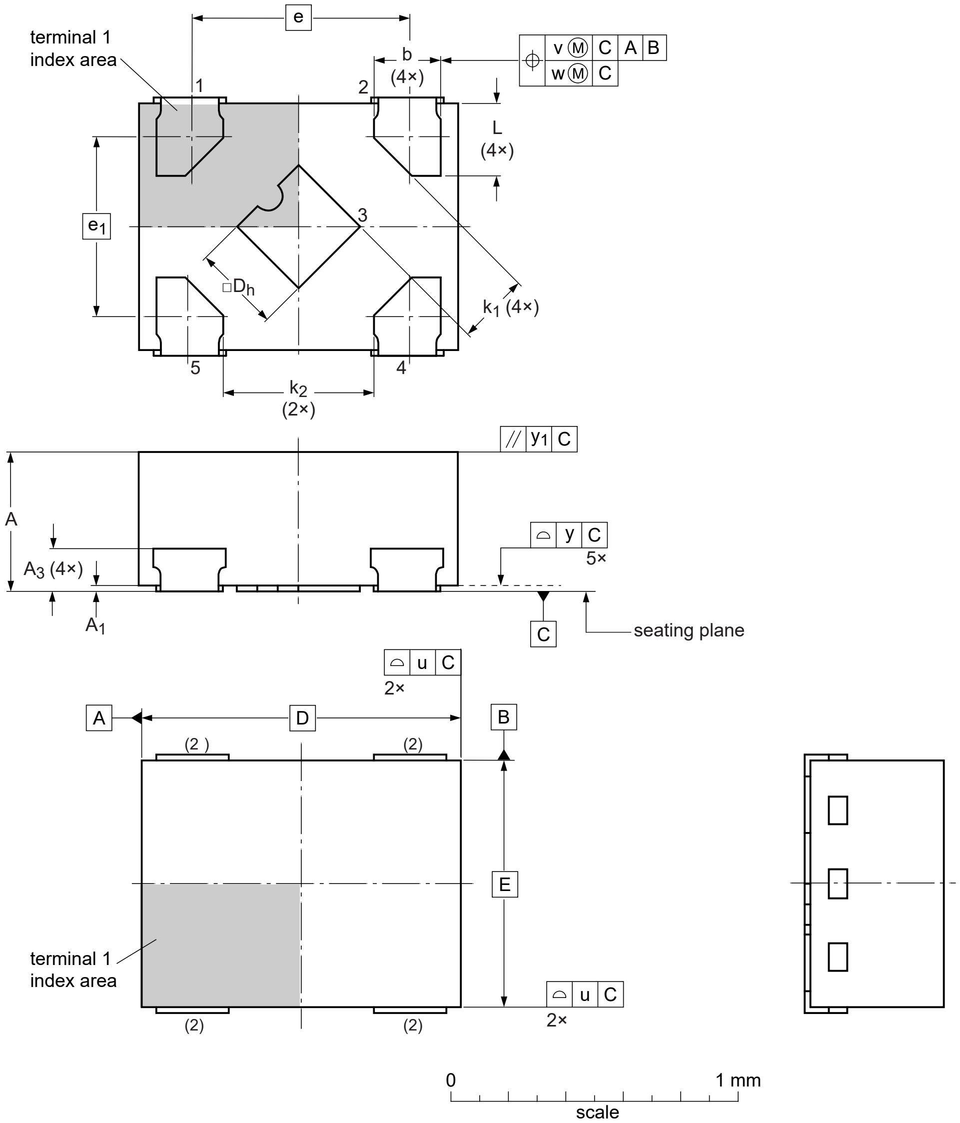
Unit		A	A_1	A_3	D	D_h	E	b	e	K	L	v	w	y	y_1
mm	max	0.35	0.04	0.10 (Typ.)	0.85	0.30	0.85	0.25			0.27	0.1	0.05	0.05	0.05
	nom	0.32	0.02		0.80	0.25	0.80	0.20	0.50		0.22				
	min	0.30	0.00		0.75	0.20	0.75	0.15		0.20	0.17				

sot1226-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	EIAJ			
SOT1226-3		- - -				~~19-11-06~~ 19-11-07

Fig. 12. Package outline SOT1226-3 (X2SON5)

XSON5: Plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm **SOT8065-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	A_3	b	$D^{(1)}$	D_h	$E^{(1)}$	e	e_1	k_1	k_2	L	u	v	w	y	y_1
mm	max	0.50	0.040		0.28		0.35						0.30					
	nom	0.47	0.020	0.135 (typ)	0.23	1.10	0.30	0.85	0.75	0.6			0.25	0.05	0.1	0.05	0.05	0.05
	min	0.44	0.005		0.20		0.27				0.2	0.45	0.22					

Note:
1. Plastic or metal protrusions per side are not included.
2. Side wettable flanks (SWF), protrusion max. 0.02 mm.

sot8065-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8065-1						~~24-05-06~~ 24-07-09

Fig. 13. Package outline SOT8065-1 (XSON5)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G125 v.17	20240711	Product data sheet	-	74LVC1G125 v.16
Modifications:	• Type number 74LVC1G125GZ (SOT8065-1/XSON5) added.			
74LVC1G125 v.16	20230823	Product data sheet	-	74LVC1G125 v.15
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74LVC1G125 v.15	20220119	Product data sheet	-	74LVC1G125 v.14
Modifications:	• Fig. 7: Package outline drawing SOT353-1 (TSSOP5) has changed.			
74LVC1G125 v.14	20211007	Product data sheet	-	74LVC1G125 v.13
Modifications:	• Section 1 and Section 2 updated. • SOT1226 (X2SON5) package changed to SOT1226-3 (X2SON5) package. • Type number 74LVC1G125GF (SOT891/XSON6) removed. • Table 5: Derating values for P_{tot} total power dissipation updated.			
74LVC1G125 v.13	20171107	Product data sheet	-	74LVC1G125 v.12
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74LVC1G125 v.12	20161202	Product data sheet	-	74LVC1G125 v.11
Modifications:	• Table 7: The maximum limits for leakage current and supply current have changed.			
74LVC1G125 v.11	20120702	Product data sheet	-	74LVC1G125 v.10
Modifications:	• Added type number 74LVC1G125GX (SOT1226) • Package outline drawing of SOT886 (Fig. 9) modified.			
74LVC1G125 v.10	20111207	Product data sheet	-	74LVC1G125 v.9
Modifications:	• Legal pages updated.			
74LVC1G125 v.9	20101229	Product data sheet	-	74LVC1G125 v.8
74LVC1G125 v.8	20100824	Product data sheet	-	74LVC1G125 v.7
74LVC1G125 v.7	20070830	Product data sheet	-	74LVC1G125 v.6
74LVC1G125 v.6	20060912	Product data sheet	-	74LVC1G125 v.5

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Contents