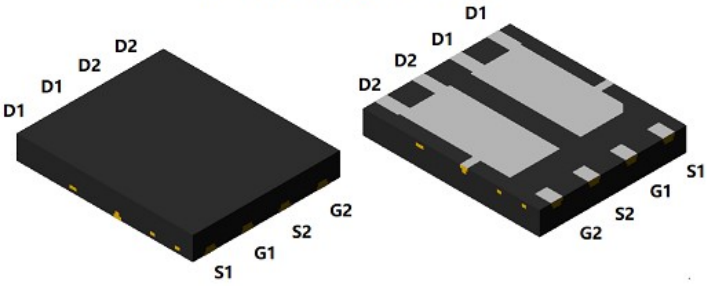
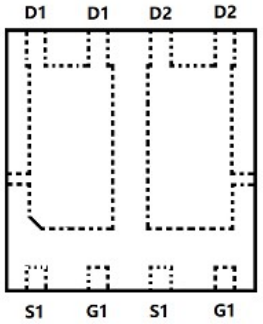
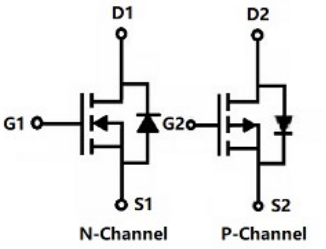
N-Channel and P-Channel Complementary Power MOSFET

DFN5x6-8L







Product Summary

NMOS(Die1)

- V_{DS} 30V
- I_D 40A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜10 mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜14 mohm

PMOS(Die2)

- V_{DS} -30V
- I_D - 40A
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜17mohm
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜27mohm

General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-source Voltage		V_{DS}	30	-30	V
Gate-source Voltage		V_{GS}	±20	±25	V
Drain Current	T_C=25℃	I_D	40	-40	A
	T_C=70℃		32	-32	
Pulsed Drain Current [A]		I_{DM}	140	-160	A
Single Pulse Avalanche Energy [B]		E_{AS}	56	72	mJ
Total Power Dissipation	T_C=25℃	P_D	21	35	W
Thermal Resistance Junction-to-Case @ Steady State [C]		$R_{\theta JC}$	6.0	3.57	℃/ W
Thermal Resistance Junction-to-Case @ Steady State [C]		$R_{\theta JA}$	25	25	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55~+150	-55~+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG40NP03A	F1	YJG40NP03A	5000	10000	100000	13“ reel

■ N-MOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=15A		8	10	mΩ
		V_{GS}= 4.5V, I_D=10A		12	14	
Diode Forward Voltage	V_{SD}	I_S=15A,V_{GS}=0V		0.85	1.2	V
Maximum Body-Diode Continuous Current	I_S				40	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=15V,V_{GS}=0V,f=1MHZ		1015		pF
Output Capacitance	C_{oss}			201		
Reverse Transfer Capacitance	C_{rss}			164		
Gate resistance	Rg	f=1MHz		2.0		Ω
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=15V,I_D=15A		23.6		nC
Gate-Source Charge	Q_{gs}			3.9		
Gate-Drain Charge	Q_{gd}			7		
Reverse Recovery Charge	Q_{rr}	I_F=25A, di/dt=100A/us		0.2		
Reverse Recovery Time	t_{rr}			5		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=20V, I_D=2A,R_L=1Ω R_{GEN}=3Ω		7		
Turn-on Rise Time	t_r			19		
Turn-off Delay Time	$t_{D(off)}$			24		
Turn-off fall Time	t_f			24		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. T_j=25℃, V_{DD}=20V, V_G=10V, L=0.5Mh.

C. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ P-MOS Electrical Characteristics (TJ=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V,T_C=25℃			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±25V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-1.2	-1.8	-2.8	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -10V, I_D=-15A		13	17	mΩ
		V_{GS}= -4.5V, I_D=-10A		17	27	
Diode Forward Voltage	V_{SD}	I_S=-15A,V_{GS}=0V			-1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-15V,V_{GS}=0V,f=1MHZ		2152		pF
Output Capacitance	C_{oss}			308		
Reverse Transfer Capacitance	C_{rss}			242		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V,V_{DS}=-15V,I_D=-12A		40.1		nC
Gate Source Charge	Q_{gs}			8.4		
Gate Drain Charge	Q_{gd}			8.6		
Reverse Recovery Charge	Q_{rr}	I_F= -12A, di/dt=100A/us		7.8		
Reverse Recovery Time	t_{rr}			18		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V,V_{DD}=-15V, I_D=-1A, R_{GEN}=2.5Ω		8		
Turn-on Rise Time	t_r			19		
Turn-off Delay Time	$t_{D(off)}$			75		
Turn-off Fall Time	t_f			46		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. T_j=25℃, V_{DD}=-20V, V_G=-10V, L=0.5Mh.

C. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ N-MOS Typical Performance Characteristics

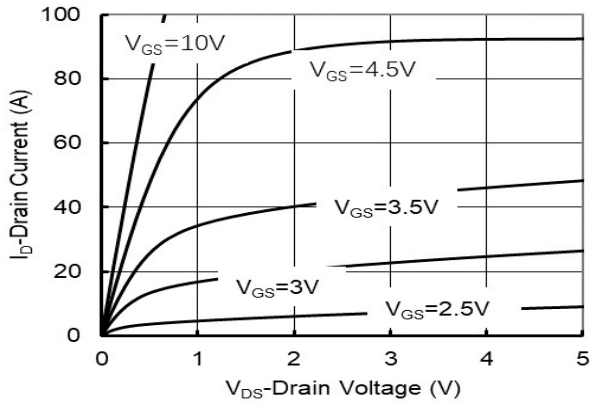


Figure1. Output Characteristics

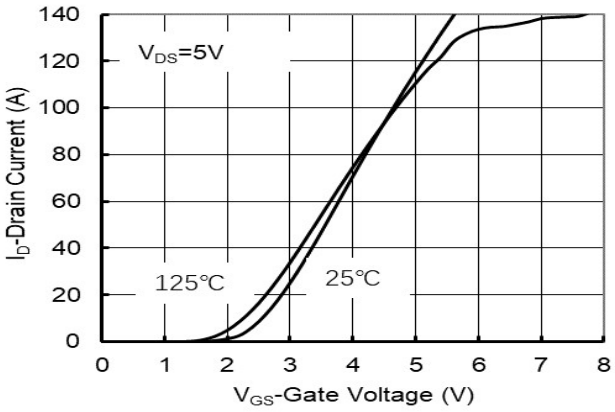


Figure2. Transfer Characteristics

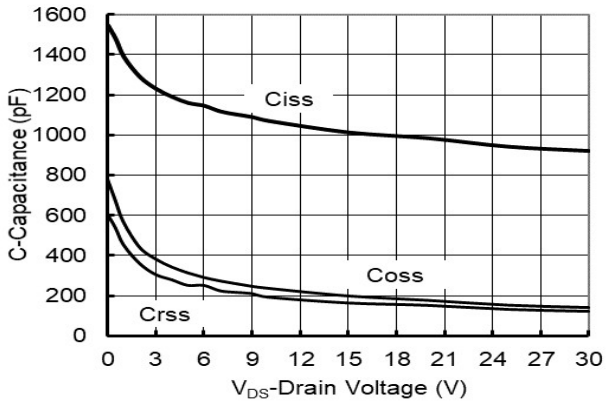


Figure3. Capacitance Characteristics

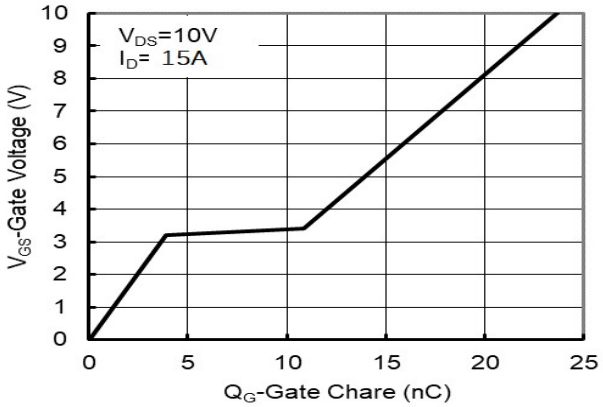


Figure4. Gate Charge

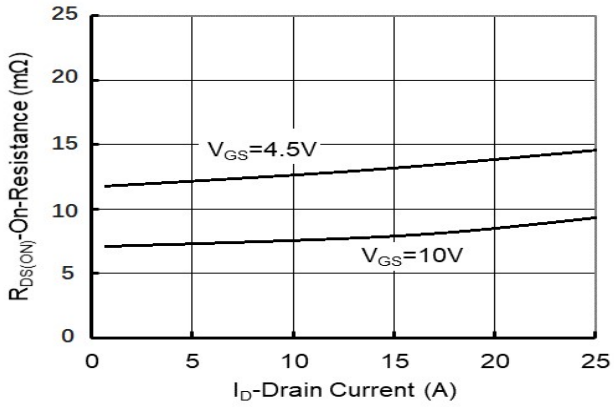


Figure5. Drain-Source on Resistance

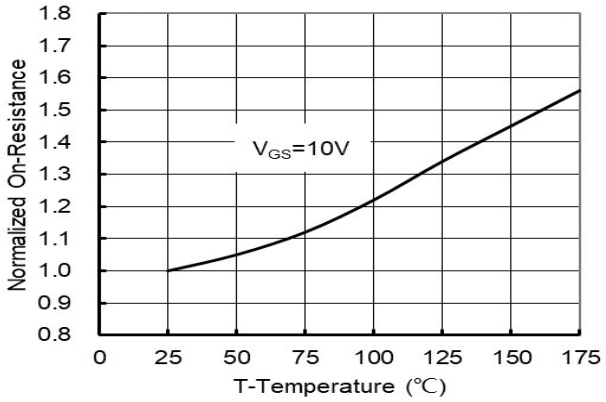


Figure6. Drain-Source on Resistance

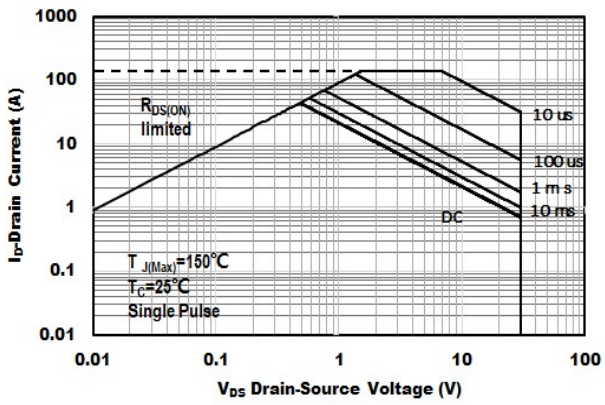


Figure7. Safe Operation Area

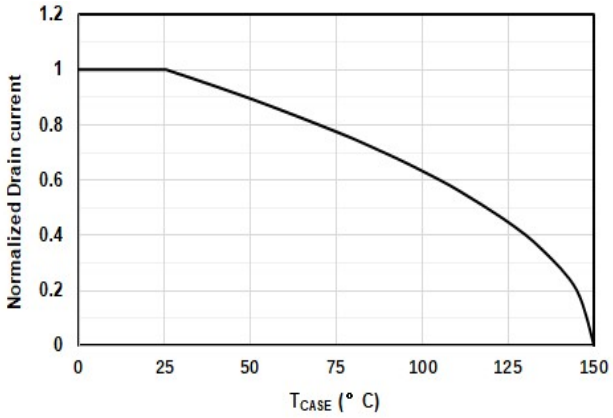


Figure8. Drain current vs. Case Temperature

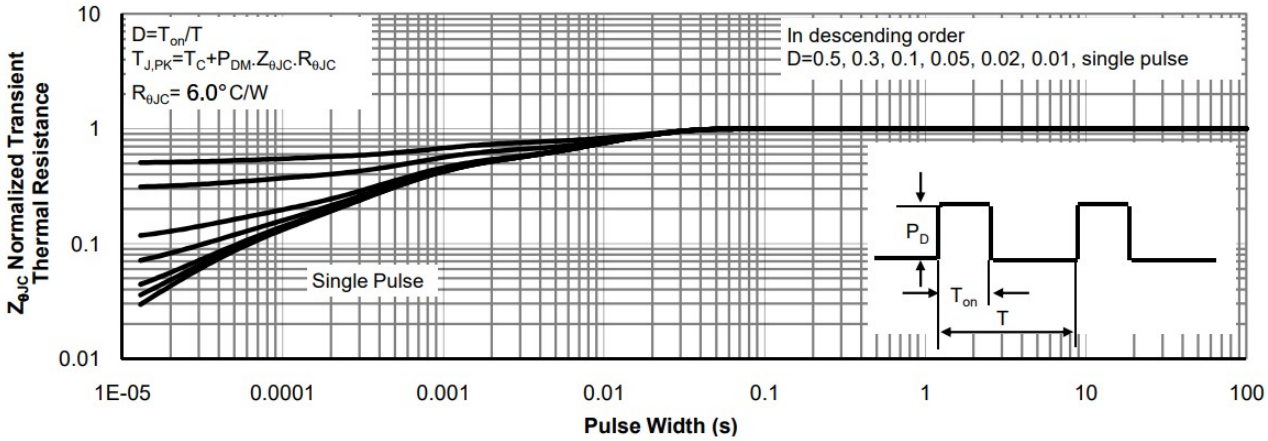


Figure 9. Normalized Maximum Transient Thermal Impedance

■ P-MOS Typical Performance Characteristics

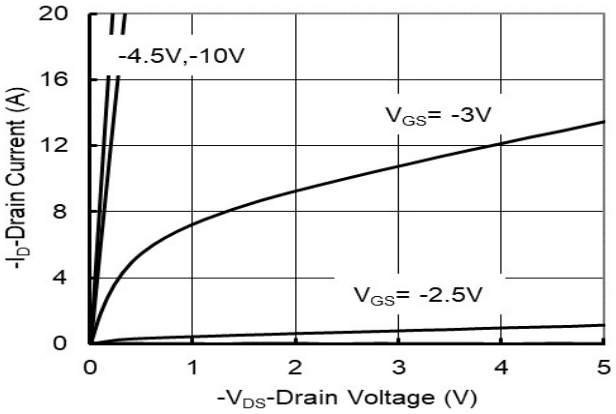


Figure1. Output Characteristics

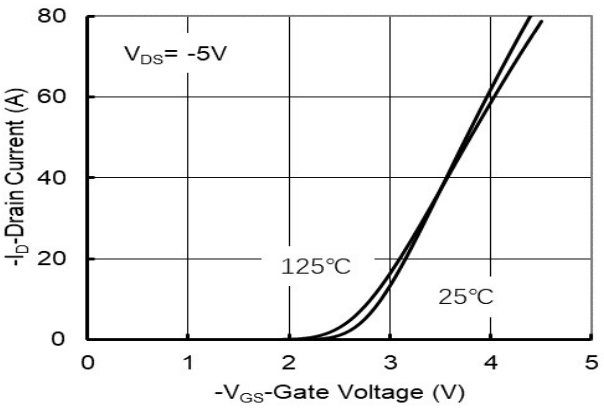


Figure2. Transfer Characteristics

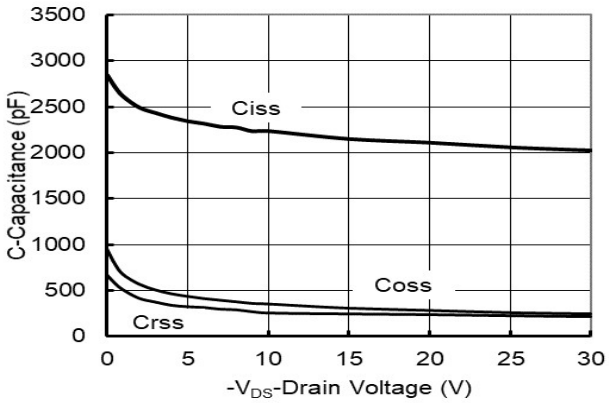


Figure3. Capacitance Characteristics

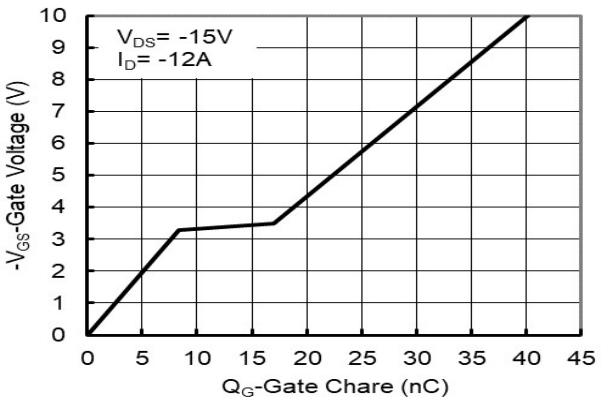


Figure4. Gate Charge

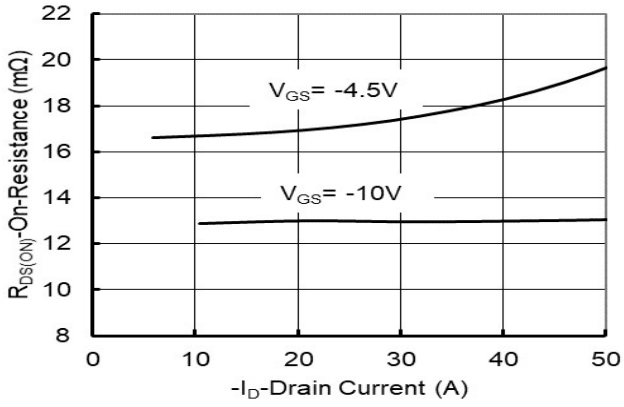


Figure5. Drain-Source on Resistance

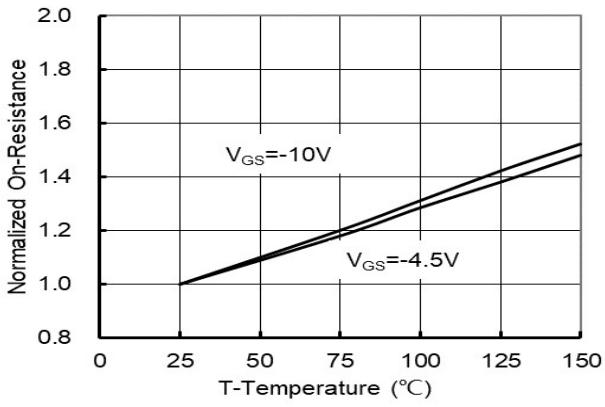


Figure6. Drain-Source on Resistance

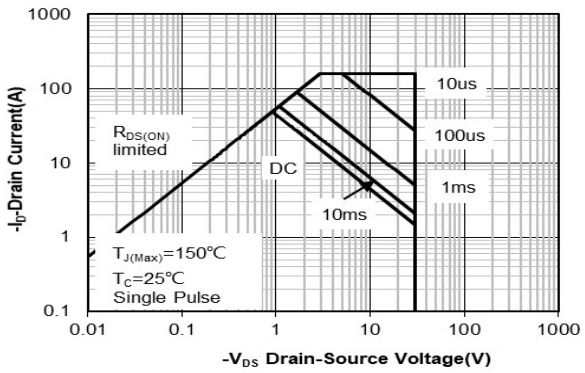


Figure7. Safe Operation Area

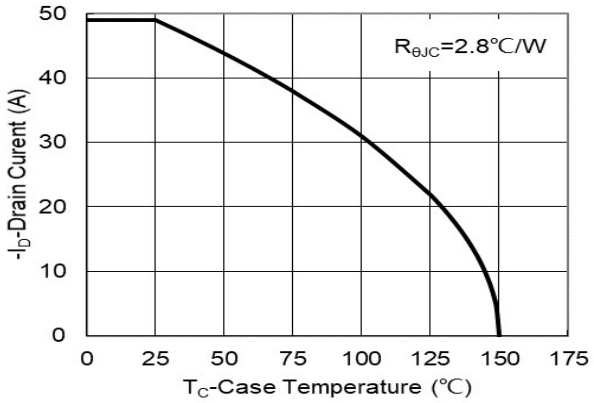


Figure8. Drain current vs. Case Temperature

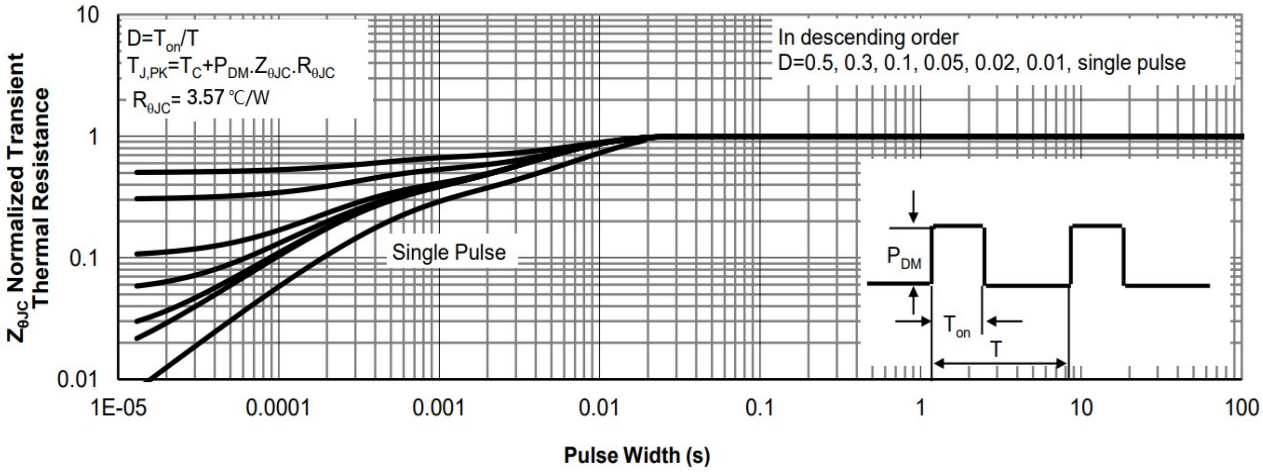
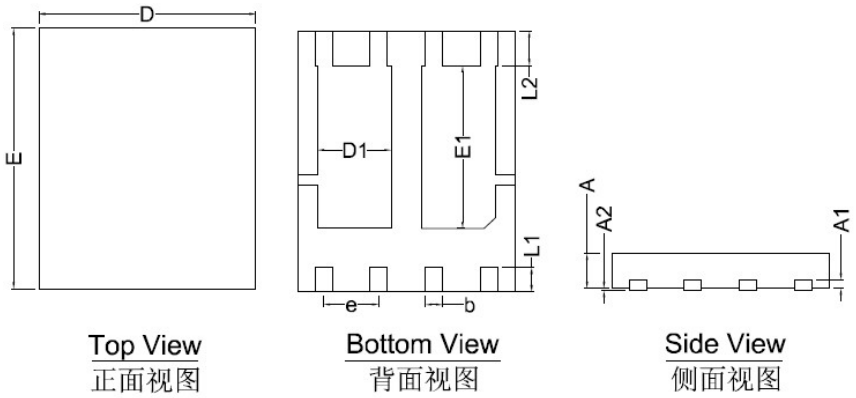


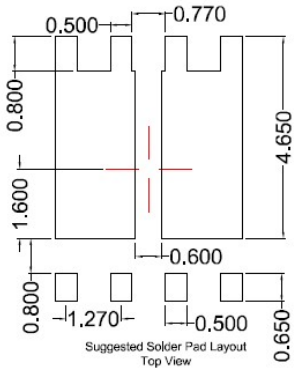
Figure 9. Normalized Maximum Transient Thermal Impedance

■ DFN5x6-8L Package Information



Top View 正面视图　　Bottom View 背面视图　　Side View 侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	4.90	5.00	5.10
E	5.90	6.00	6.10
A	0.70	0.80	0.90
A1		0.20 BSC	
A2			0.10
D1	1.60	1.70	1.80
E1	3.65	3.75	3.85
L1	0.45	0.55	0.65
L2		0.80 BSC	
b	0.30	0.40	0.50
e		1.27 BSC	



Suggested Solder Pad Layout
Top View

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

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