



0.05 $\mu\text{V}/^\circ\text{C}$ max, SINGLE-SUPPLY CMOS OPERATIONAL AMPLIFIERS Zero-Drift Series

FEATURES

- LOW OFFSET VOLTAGE: 5 μV (max)
- ZERO DRIFT: 0.05 $\mu\text{V}/^\circ\text{C}$ (max)
- QUIESCENT CURRENT: 285 μA
- SINGLE-SUPPLY OPERATION
- SINGLE AND DUAL VERSIONS
- SHUTDOWN
- *Micro*SIZE PACKAGES

APPLICATIONS

- TRANSDUCER APPLICATIONS
- TEMPERATURE MEASUREMENT
- ELECTRONIC SCALES
- MEDICAL INSTRUMENTATION
- BATTERY-POWERED INSTRUMENTS
- HANDHELD TEST EQUIPMENT

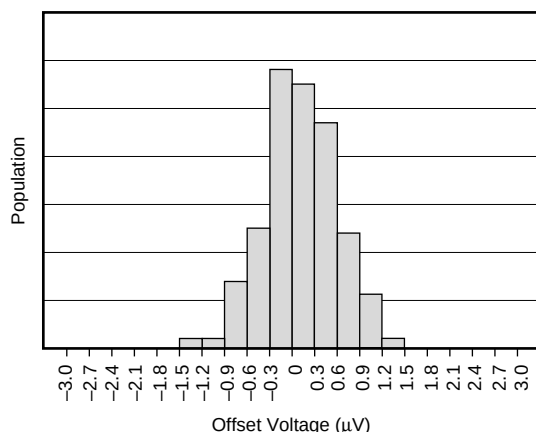
DESCRIPTION

The OPA334 and OPA335 series of CMOS operational amplifiers use auto-zeroing techniques to simultaneously provide very low offset voltage (5 μV max), and near-zero drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high input impedance and rail-to-rail output swing. Single or dual supplies as low as +2.7V ($\pm 1.35\text{V}$) and up to +5.5V ($\pm 2.75\text{V}$) may be used. These op amps are optimized for low-voltage, single-supply operation.

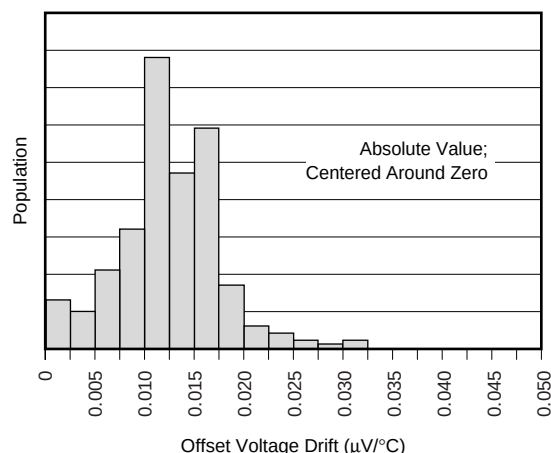
The OPA334 family includes a shutdown mode. Under logic control, the amplifiers can be switched from normal operation to a standby current of 2 μA . When the Enable pin is connected high, the amplifier is active. Connecting Enable low disables the amplifier, and places the output in a high-impedance state.

The OPA334 (single version with shutdown) comes in *Micro*SIZE SOT23-6. The OPA335 (single version without shutdown) is available in SOT23-5, and SO-8. The OPA2334 (dual version with shutdown) comes in *Micro*SIZE MSOP-10. The OPA2335 (dual version without shutdown) is offered in the MSOP-8 and SO-8 packages. All versions are specified for operation from -40°C to $+125^\circ\text{C}$.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION



OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage	+7V
Signal Input Terminals, Voltage ⁽²⁾	–0.5V to (V+) + 0.5V
Current ⁽²⁾	±10mA
Output Short Circuit ⁽³⁾	Continuous
Operating Temperature	–40°C to +150°C
Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these, or any other conditions beyond those specified, is not implied. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

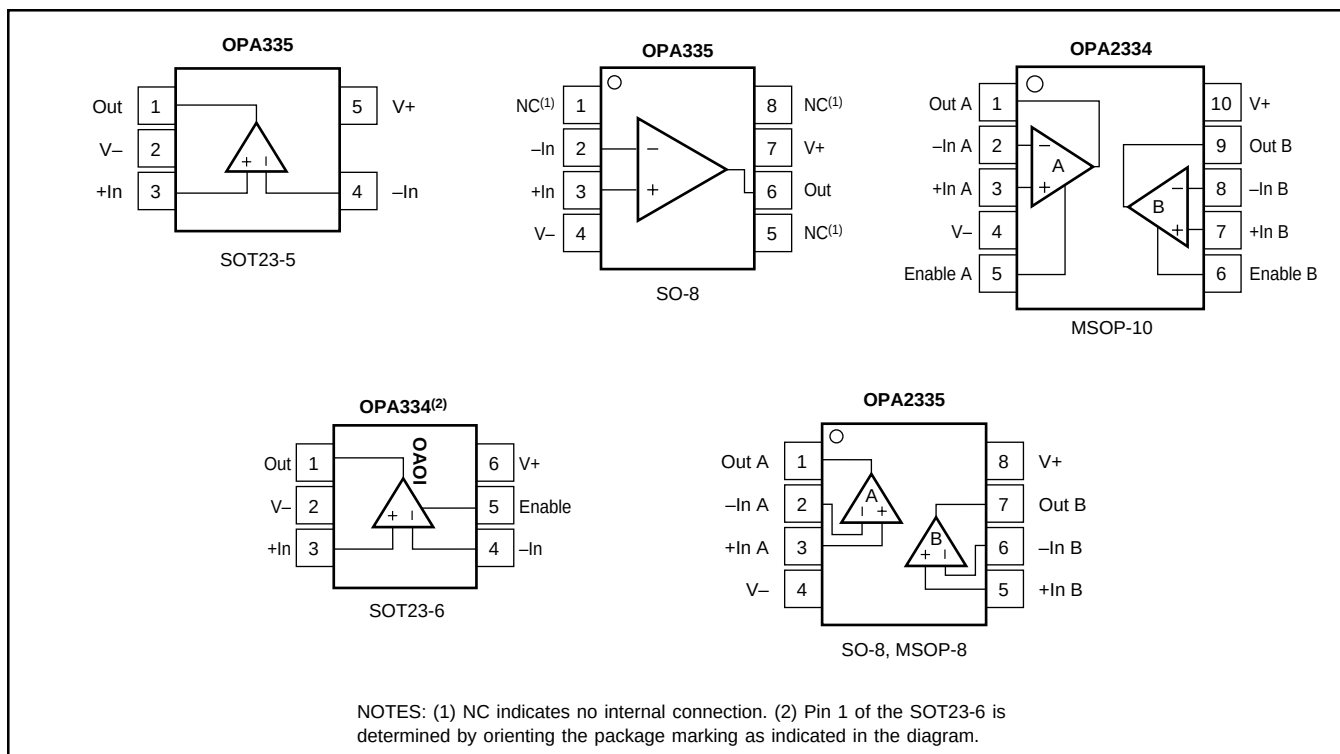
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR ⁽¹⁾	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
Shutdown Version						
OPA334	SOT23-6	DBV	–40°C to +125°C	OA0I	OPA334AIDBVT	Tape and Reel, 250
"	"	"	"	"	OPA334AIDBVR	Tape and Reel, 3000
OPA2334	MSOP-10	DGS	–40°C to +125°C	BHE	OPA2334AIDGST	Tape and Reel, 250
"	"	"	"	"	OPA2334AIDGSR	Tape and Reel, 2500
Non-Shutdown Version						
OPA335	SOT23-5	DBV	–40°C to +125°C	OAPI	OPA335AIDBVT	Tape and Reel, 250
"	"	"	"	"	OPA335AIDBVR	Tape and Reel, 3000
OPA335	SO-8	D	–40°C to +125°C	OPA335	OPA335AID	Rails, 100
"	"	"	"	"	OPA335AIDR	Tape and Reel, 2500
OPA2335	SO-8	D	–40°C to +125°C	OPA2335	OPA2335AID	Rails, 100
"	"	"	"	"	OPA2335AIDR	Tape and Reel, 2500
OPA2335	MSOP-8	DGK	–40°C to +125°C	BHF	OPA2335AIDGKT	Tape and Reel, 250
"	"	"	"	"	OPA2335AIDGKR	Tape and Reel, 2500

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

PIN CONFIGURATIONS



ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$.

At $T_A = +25^{\circ}\text{C}$, $V_S = +5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

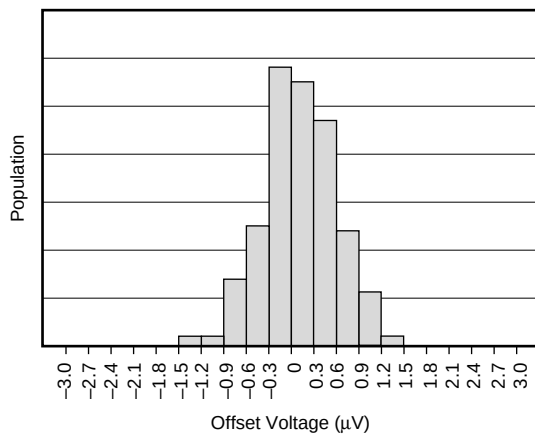
PARAMETER	CONDITION	OPA334AI, OPA335AI OPA2334AI, OPA2335AI			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage V_{OS} vs Temperature dV_{OS}/dT vs Power Supply PSRR Long-Term Stability ⁽¹⁾ Channel Separation, dc	$V_{CM} = V_S/2$ $V_S = +2.7\text{V}$ to $+5.5\text{V}$, $V_{CM} = 0$, Over Temperature		1 ± 0.02 ± 1 See Note (1) 0.1	5 ± 0.05 ± 2	μV $\mu\text{V}/^{\circ}\text{C}$ $\mu\text{V/V}$ $\mu\text{V/V}$
INPUT BIAS CURRENT Input Bias Current I_B Over Temperature Input Offset Current I_{OS}	$V_{CM} = V_S/2$		± 70 1 ± 120	± 200 ± 400	pA nA pA
NOISE Input Voltage Noise, $f = 0.01\text{Hz}$ to 10Hz e_n Input Current Noise Density, $f = 10\text{Hz}$ i_n			1.4 20		μV_{PP} $\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE Common-Mode Voltage Range V_{CM} Common-Mode Rejection Ratio CMRR	$(V-) - 0.1\text{V} < V_{CM} < (V+) - 15\text{V}$, Over Temperature	$(V-) - 0.1$ 110	130	$(V+) - 1.5$	V dB
INPUT CAPACITANCE Differential Common-Mode			1 5		pF pF
OPEN-LOOP GAIN Open-Loop Voltage Gain, Over Temperature A_{OL} Over Temperature	$50\text{mV} < V_O < (V+) - 50\text{mV}$, $R_L = 100\text{k}\Omega$, $V_{CM} = V_S/2$ $100\text{mV} < V_O < (V+) - 100\text{mV}$, $R_L = 10\text{k}\Omega$, $V_{CM} = V_S/2$	110 110	130 130		dB dB
FREQUENCY RESPONSE Gain-Bandwidth Product GBW Slew Rate SR	$G = +1$		2 1.6		MHz V/ μs
OUTPUT Voltage Output Swing from Rail Voltage Output Swing from Rail Short-Circuit Current I_{SC} Capacitive Load Drive C_{LOAD}	$R_L = 10\text{k}\Omega$, Over Temperature $R_L = 100\text{k}\Omega$, Over Temperature		15 1 ± 50	100 50	mV mV mA
See Typical Characteristics					
SHUTDOWN t_{OFF} $t_{ON}^{(2)}$ V_L (shutdown) V_H (amplifier is active) Input Bias Current of Enable Pin I_{QSD}		0 0.75 (V+)	1 150 50	+0.8 5.5 2	μs μs V V pA μA
POWER SUPPLY Operating Voltage Range Quiescent Current: OPA334, OPA335 I_Q Over Temperature OPA2334, OPA2335 (total—two amplifiers) Over Temperature	$I_O = 0$ $I_O = 0$	2.7	285 570	5.5 350 450 700 900	V μA μA μA μA
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance θ_{JA} SOT23-5, SOT23-6 Surface-Mount MSOP-8, MSOP-10, SO-8 Surface-Mount		-40 -40 -65		+125 +150 +150	$^{\circ}\text{C}$ $^{\circ}\text{C}$ $^{\circ}\text{C}$ $^{\circ}\text{C/W}$ $^{\circ}\text{C/W}$ $^{\circ}\text{C/W}$

NOTES: (1) 500-hour life test at 150°C demonstrated randomly distributed variation approximately equal to measurement repeatability of $1\mu\text{V}$. (2) Device requires one complete cycle to return to V_{OS} accuracy.

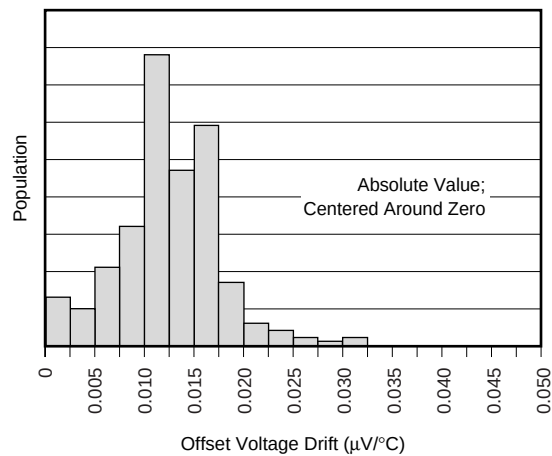
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

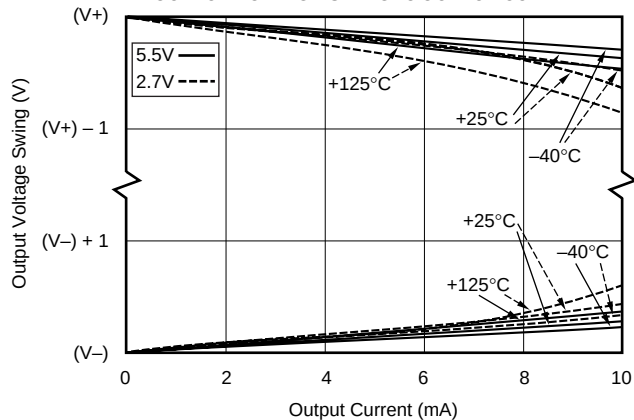
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



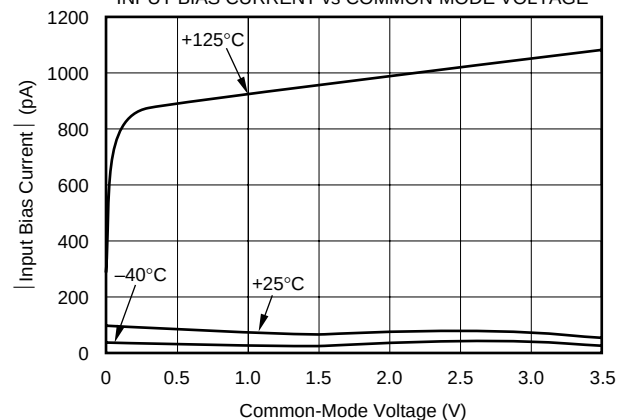
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



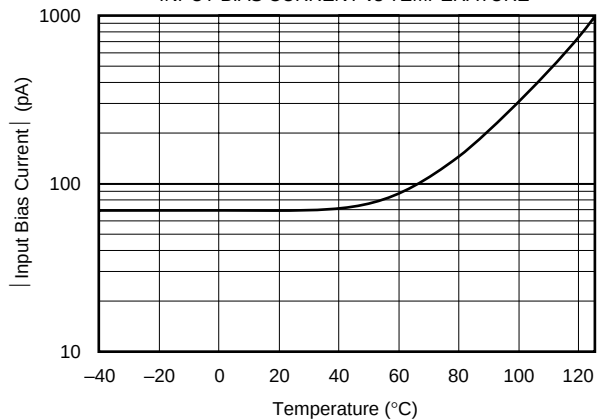
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



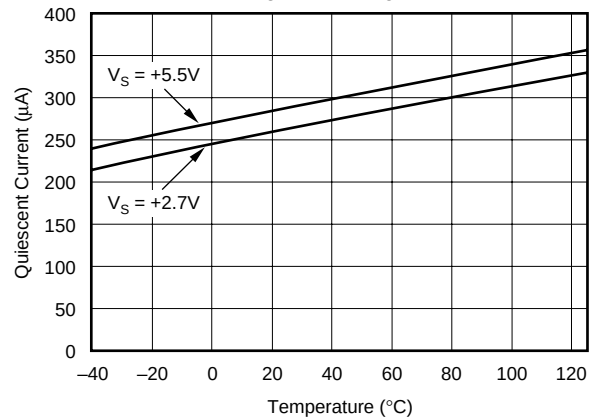
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



INPUT BIAS CURRENT vs TEMPERATURE

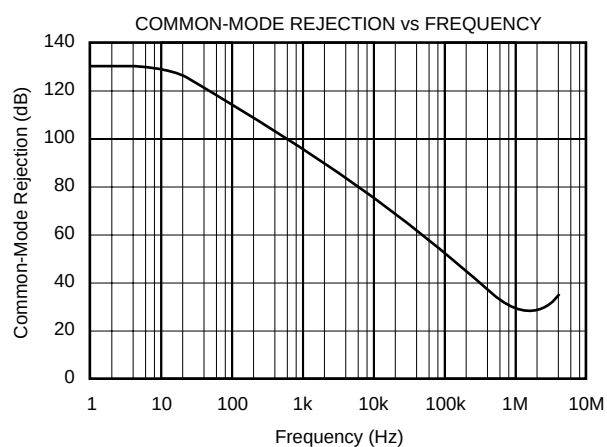
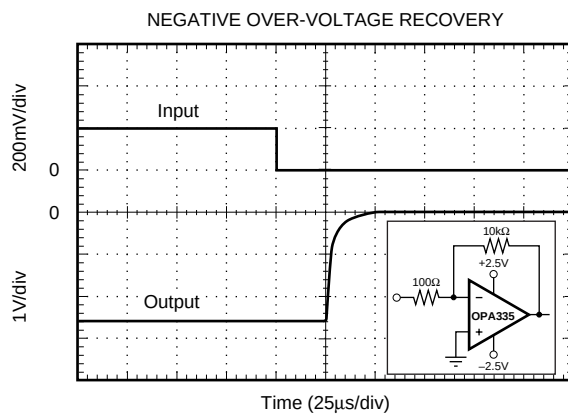
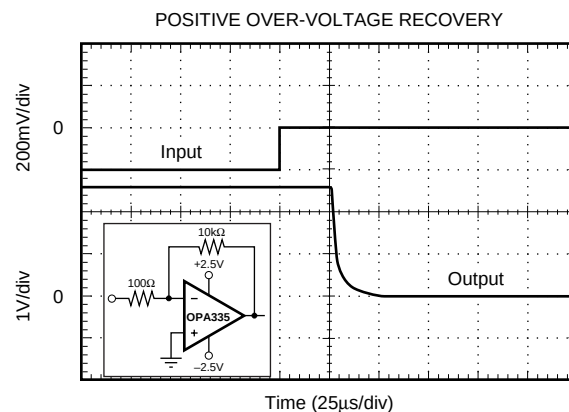
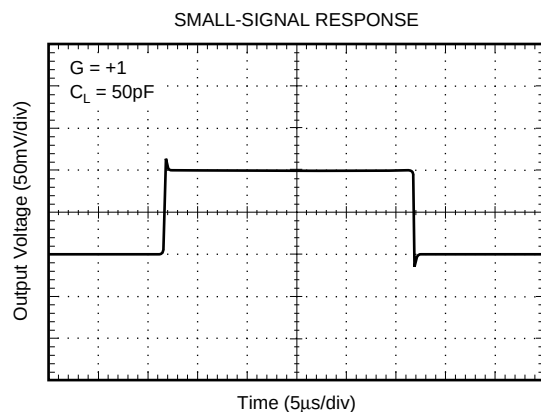
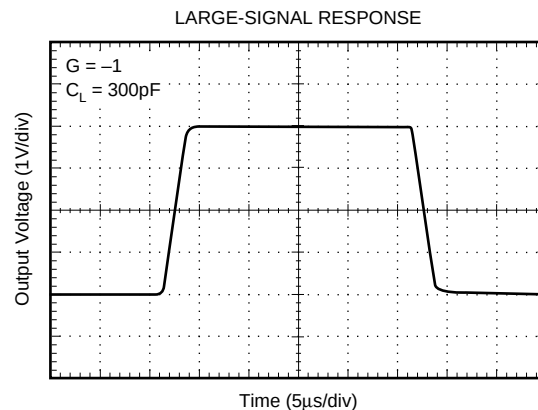
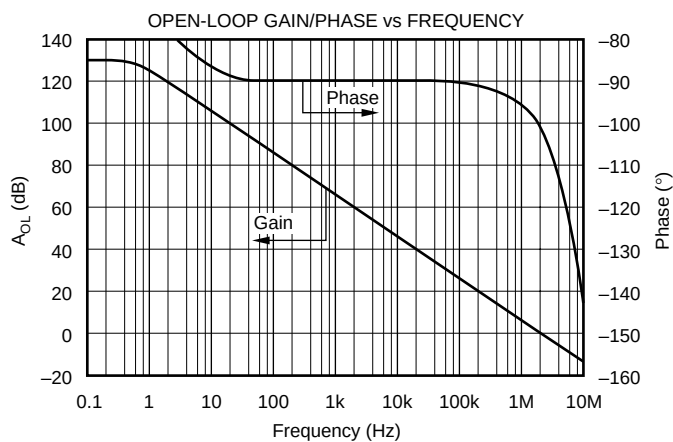


QUIESCENT CURRENT (per channel)
vs TEMPERATURE



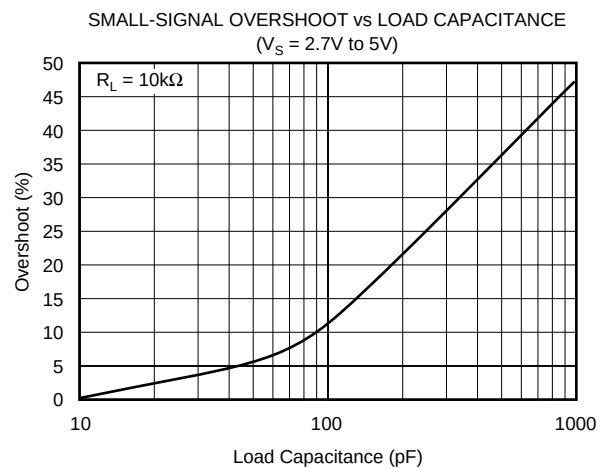
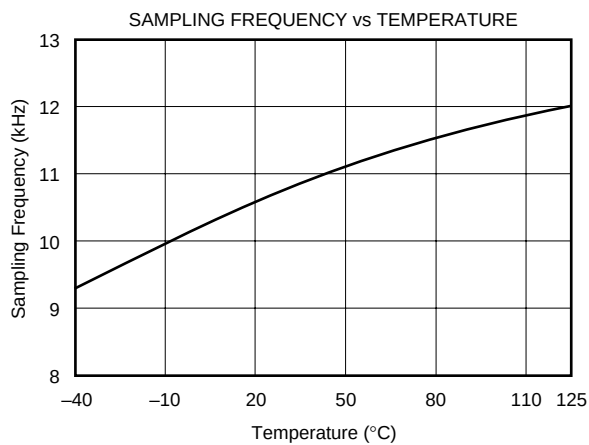
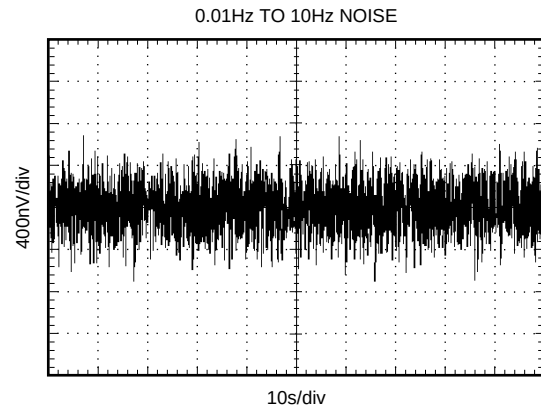
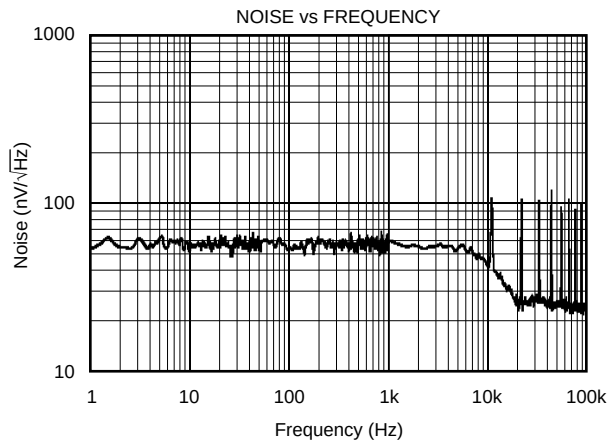
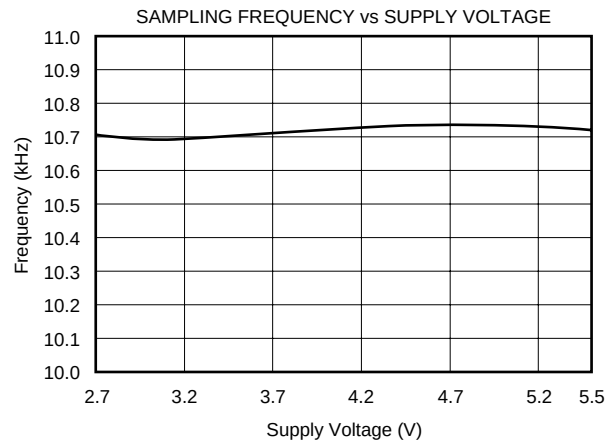
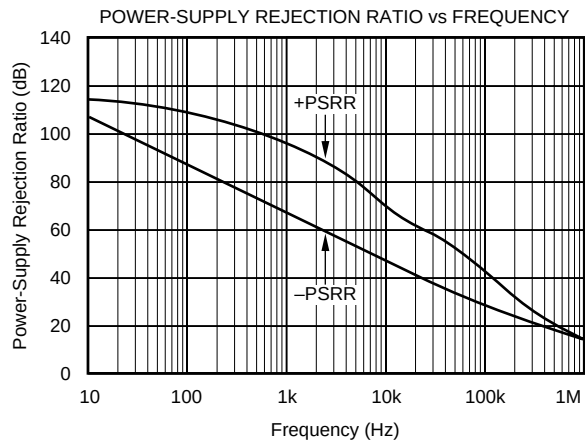
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.



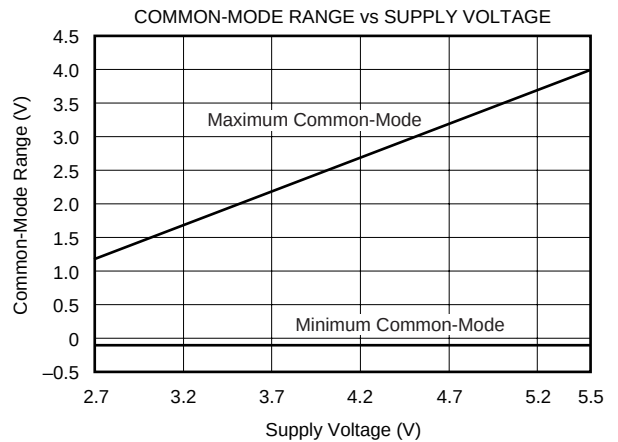
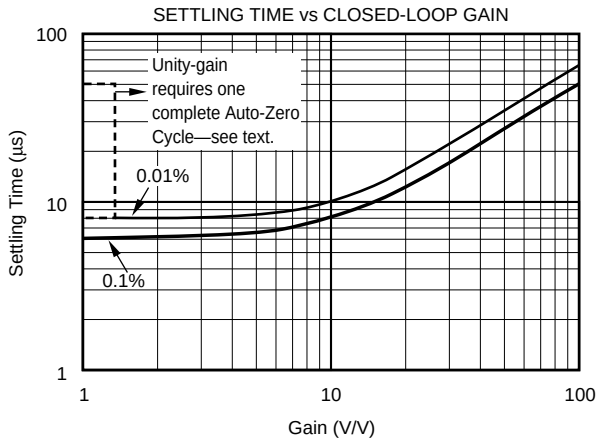
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.



TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.



APPLICATIONS INFORMATION

The OPA334 and OPA335 series op amps are unity-gain stable and free from unexpected output phase reversal. They use auto-zeroing techniques to provide low offset voltage and very low drift over time and temperature.

Good layout practice mandates use of a $0.1\mu\text{F}$ capacitor placed closely across the supply pins.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals.

- Use low thermoelectric-coefficient connections (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat-sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of $0.1\mu\text{V}/^\circ\text{C}$ or higher, depending on materials used.

OPERATING VOLTAGE

The OPA334 and OPA335 series op amps operate over a power-supply range of $+2.7\text{V}$ to $+5.5\text{V}$ ($\pm 1.35\text{V}$ to $\pm 2.75\text{V}$). Supply voltages higher than 7V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

OPA334 ENABLE FUNCTION

The enable/shutdown digital input is referenced to the V_- supply voltage of the amp. A logic high enables the op amp. A valid logic high is defined as $> 75\%$ of the total supply voltage. The valid logic high signal can be up to 5.5V above the negative supply, independent of the positive supply voltage. A valid logic low is defined as $< 0.8\text{V}$ above the V_- supply pin. If dual or split power supplies are used, be sure that logic input signals are properly referred to the negative supply voltage. The Enable pin must be connected to a valid high or low voltage, or driven, not left open circuit.

The logic input is a high-impedance CMOS input, with separate logic inputs provided on the dual version. For battery-operated applications, this feature can be used to greatly reduce the average current and extend battery life.

The enable time is $150\mu\text{s}$, which includes one full auto-zero cycle required by the amplifier to return to V_{OS} accuracy. Prior to this time, the amplifier functions properly, but with unspecified offset voltage.

Disable time is $1\mu\text{s}$. When disabled, the output assumes a high-impedance state. This allows the OPA334 to be operated as a gated amplifier, or to have the output multiplexed onto a common analog output bus.

INPUT VOLTAGE

The input common-mode range extends from $(V_-) - 0.1\text{V}$ to $(V_+) - 1.5\text{V}$. For normal operation, the inputs must be limited to this range. The common-mode rejection ratio is only valid within the valid input common-mode range. A lower supply voltage results in lower input common-mode range; therefore, attention to these values must be given when selecting the input bias voltage. For example, when operating on a single 3V power supply, common-mode range is from 0.1V below ground to half the power-supply voltage.

Normally, input bias current is approximately 70pA; however, input voltages exceeding the power supplies can cause excessive current to flow in or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10mA. This is easily accomplished with an input resistor, as shown in Figure 1.

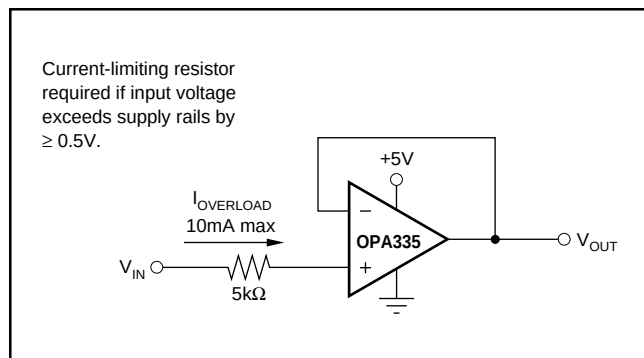


FIGURE 1. Input Current Protection.

INTERNAL OFFSET CORRECTION

The OPA334 and OPA335 series op amps use an auto-zero topology with a time-continuous 2MHz op amp in the signal path. This amplifier is zero-corrected every 100μs using a proprietary technique. Upon power-up, the amplifier requires one full auto-zero cycle of approximately 100μs to achieve specified V_{OS} accuracy. Prior to this time, the amplifier functions properly but with unspecified offset voltage.

This design has remarkably little aliasing and noise. Zero correction occurs at a 10kHz rate, but there is virtually no fundamental noise energy present at that frequency. For all practical purposes, any glitches have energy at 20MHz or higher and are easily filtered, if required. Most applications are not sensitive to such high-frequency noise, and no filtering is required.

Unity-gain operation demands that the auto-zero circuitry correct for common-mode rejection errors of the main amplifier. Because these errors can be larger than 0.01% of a full-scale input step change, one calibration cycle (100μs) can be required to achieve full accuracy. This behavior is shown in the typical characteristic section, see *Settling Time vs Closed-Loop Gain*.

ACHIEVING OUTPUT SWING TO THE OP AMP'S NEGATIVE RAIL

Some applications require output voltage swing from 0V to a positive full-scale voltage (such as +2.5V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0V, near the lower output

swing limit of a single-supply op amp. A good single-supply op amp may swing close to single-supply ground, but will not reach ground. The output of the OPA334 or OPA335 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires use of another resistor and an additional, more negative, power supply than the op amp's negative supply. A pull-down resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve, as shown in Figure 2.

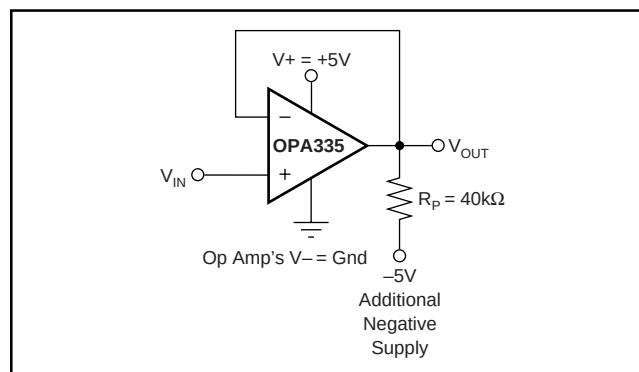


FIGURE 2. Op Amp with Pull-Down Resistor to Achieve $V_{OUT} = \text{Ground}$.

The OPA334 and OPA335 have an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below using the above technique. This technique only works with some types of output stages. The OPA334 and OPA335 have been characterized to perform well with this technique. Accuracy is excellent down to 0V and as low as -2mV. Limiting and non-linearity occurs below -2mV, but excellent accuracy returns as the output is again driven above -2mV. Lowering the resistance of the pull-down resistor will allow the op amp to swing even further below the negative rail. Resistances as low as 10kΩ can be used to achieve excellent accuracy down to -10mV.

LAYOUT GUIDELINES

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1μF capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI (electromagnetic-interference) susceptibility.

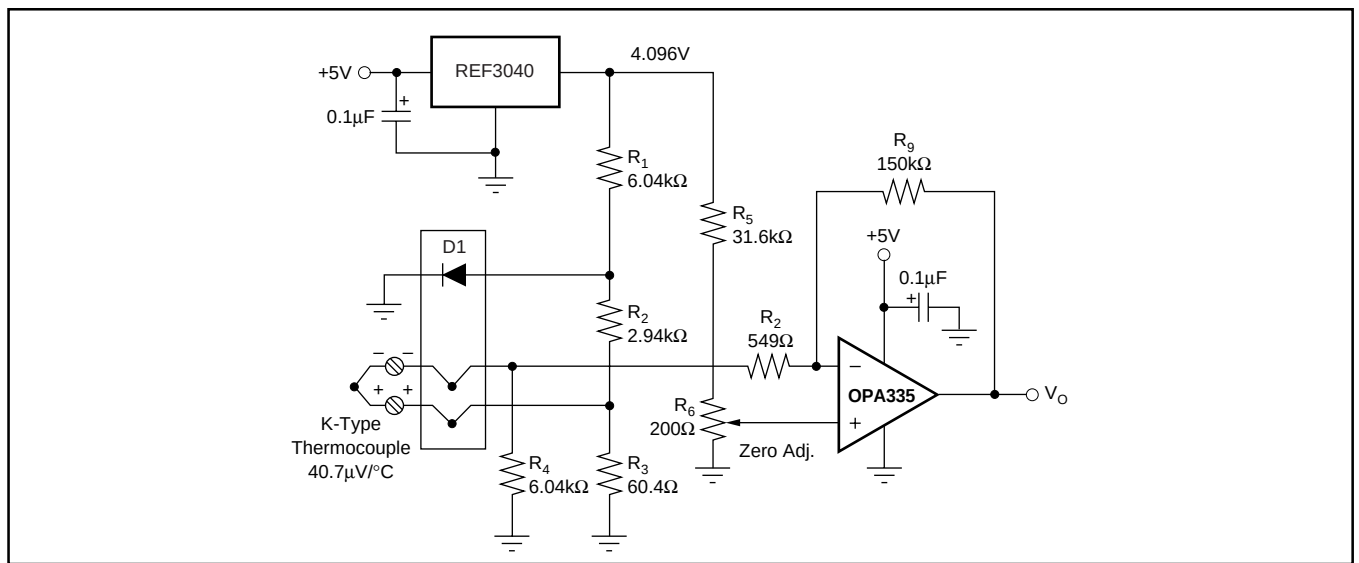


FIGURE 3. Temperature Measurement Circuit.

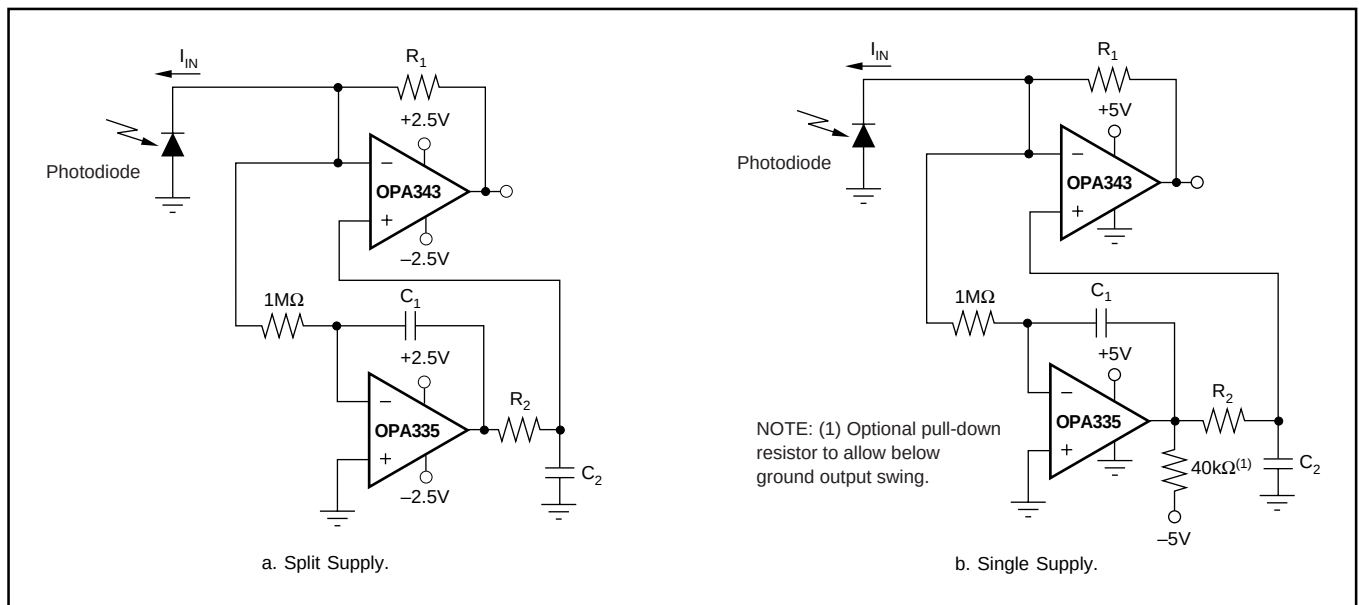


FIGURE 4. Auto-Zeroed Transimpedance Amplifier.

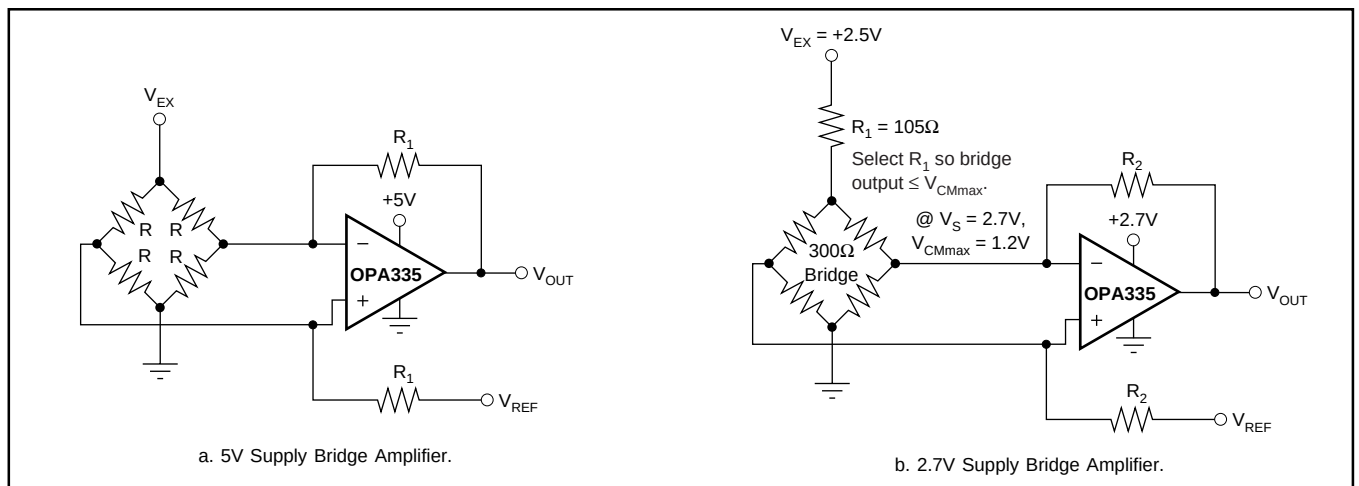


FIGURE 5. Single Op Amp Bridge Amplifier Circuits.

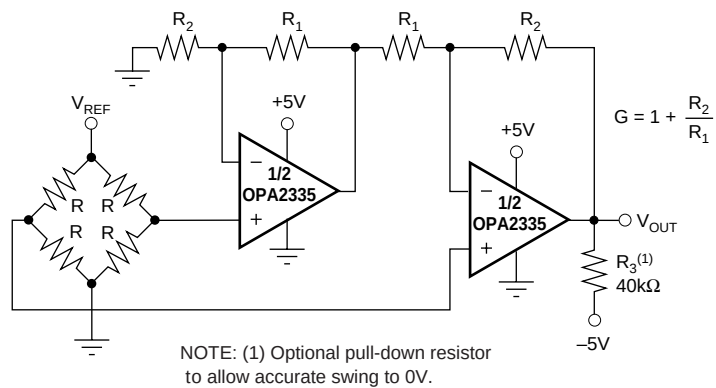


FIGURE 6. Dual Op Amp IA Bridge Amplifier.

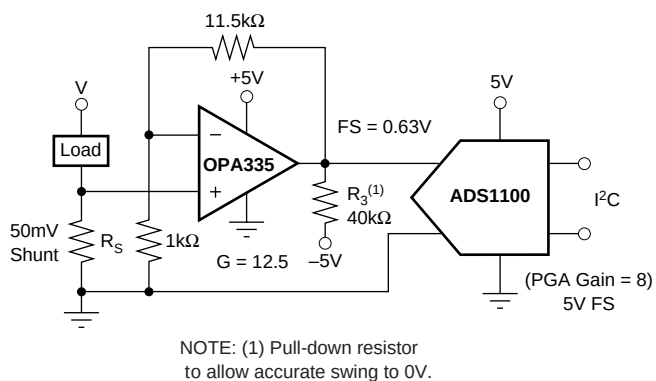


FIGURE 7. Low-Side Current Measurement.

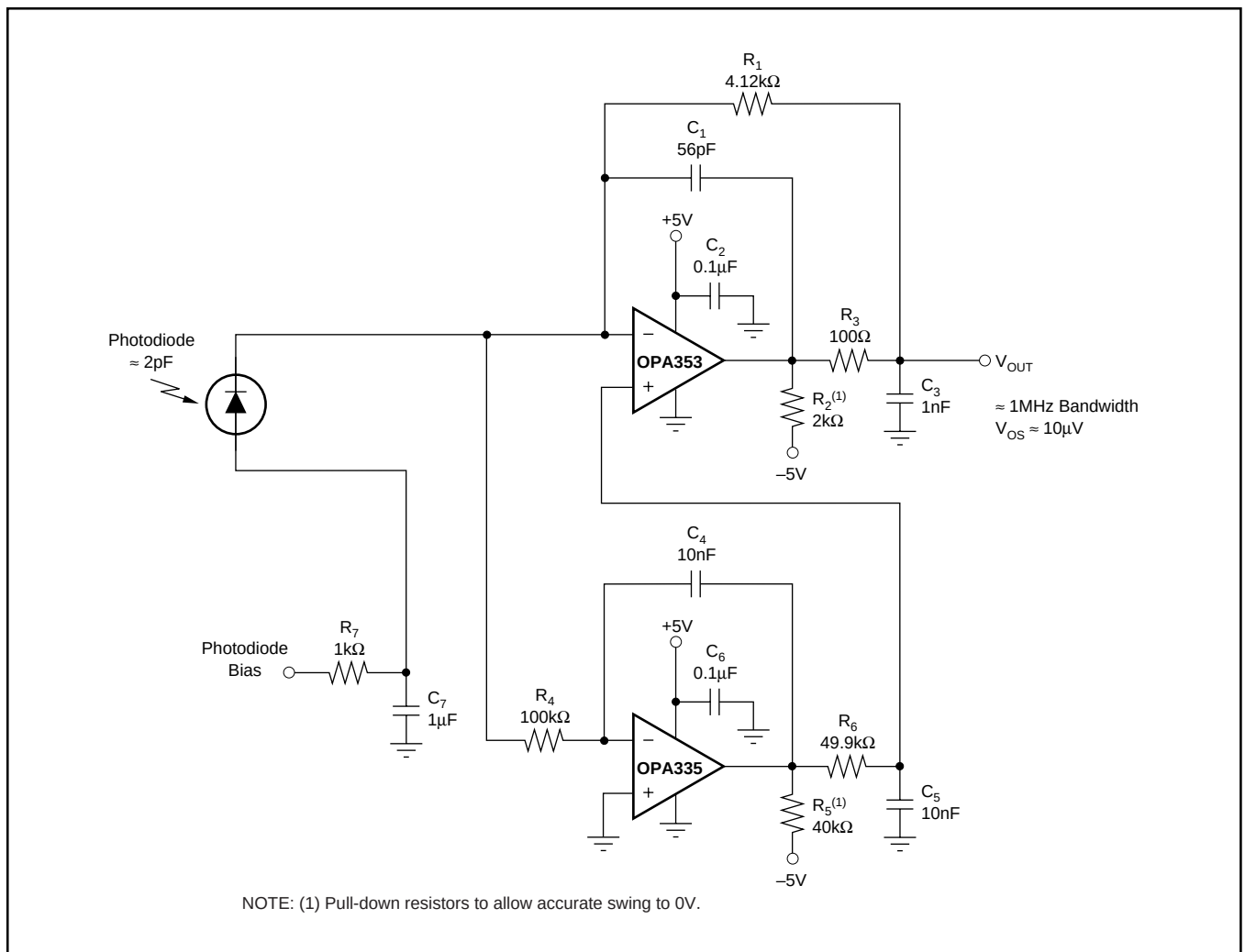
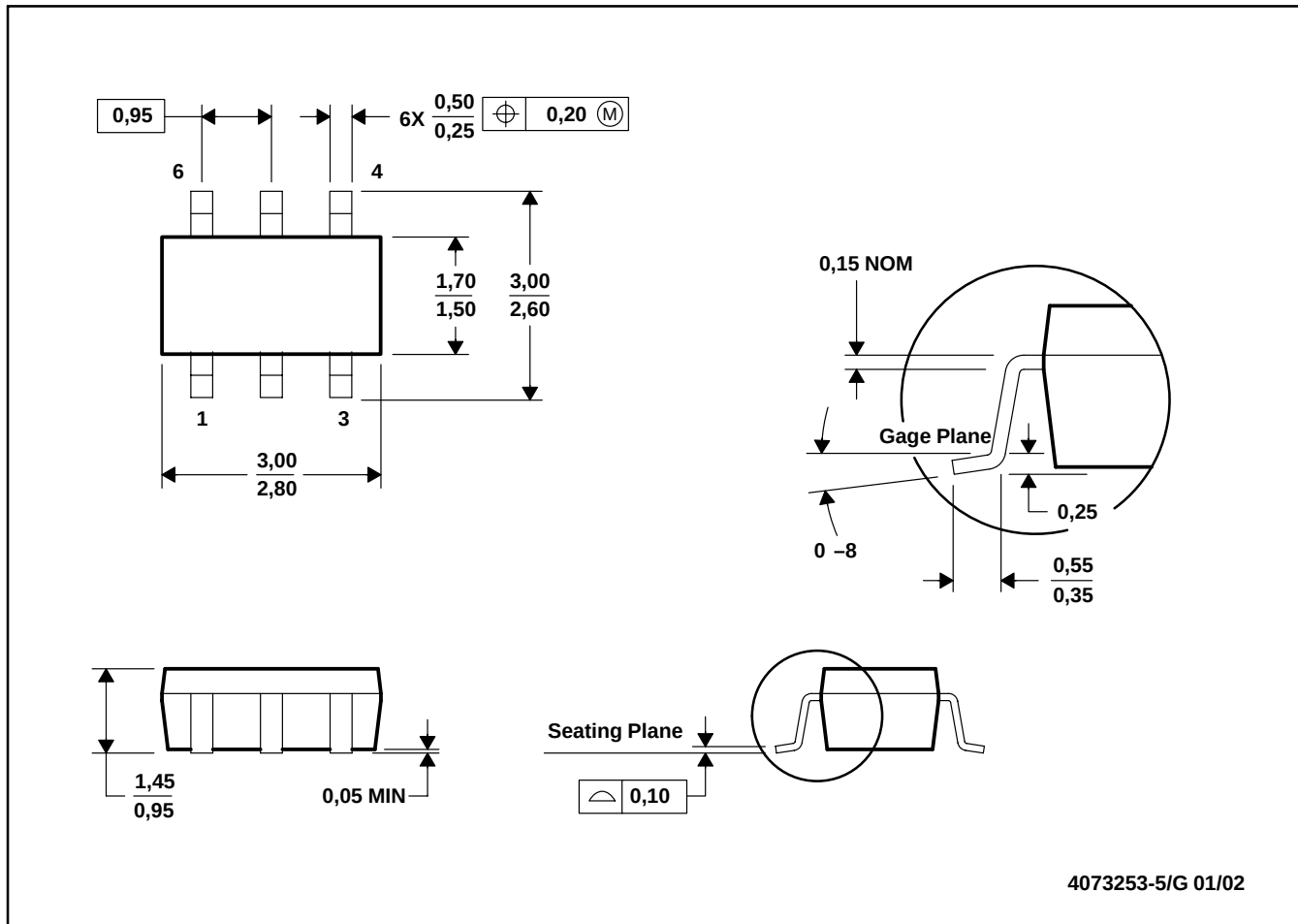
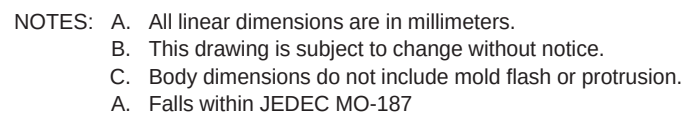
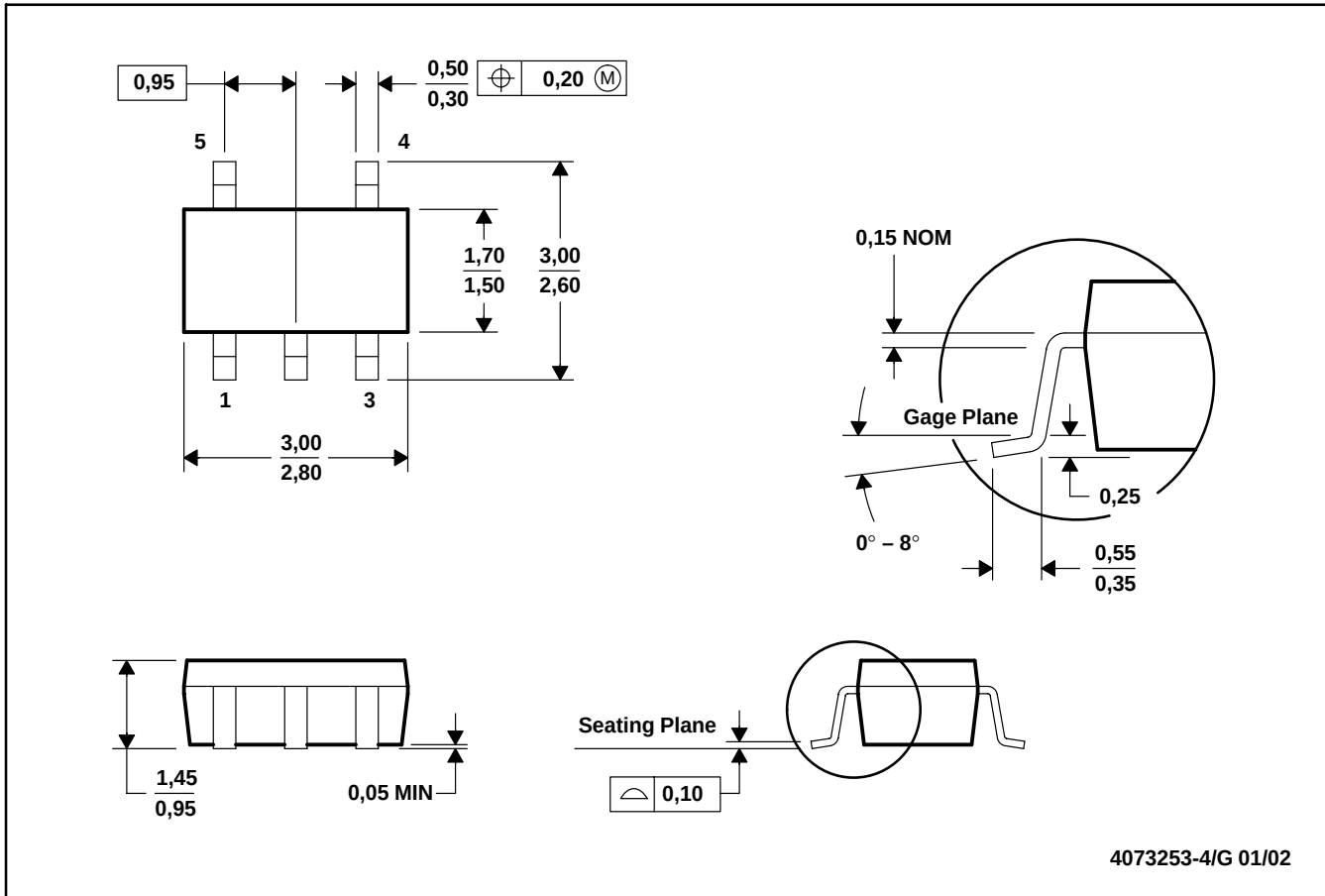


FIGURE 8. High Dynamic Range Transimpedance Amplifier.



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.

PLASTIC SMALL-OUTLINE PACKAGE

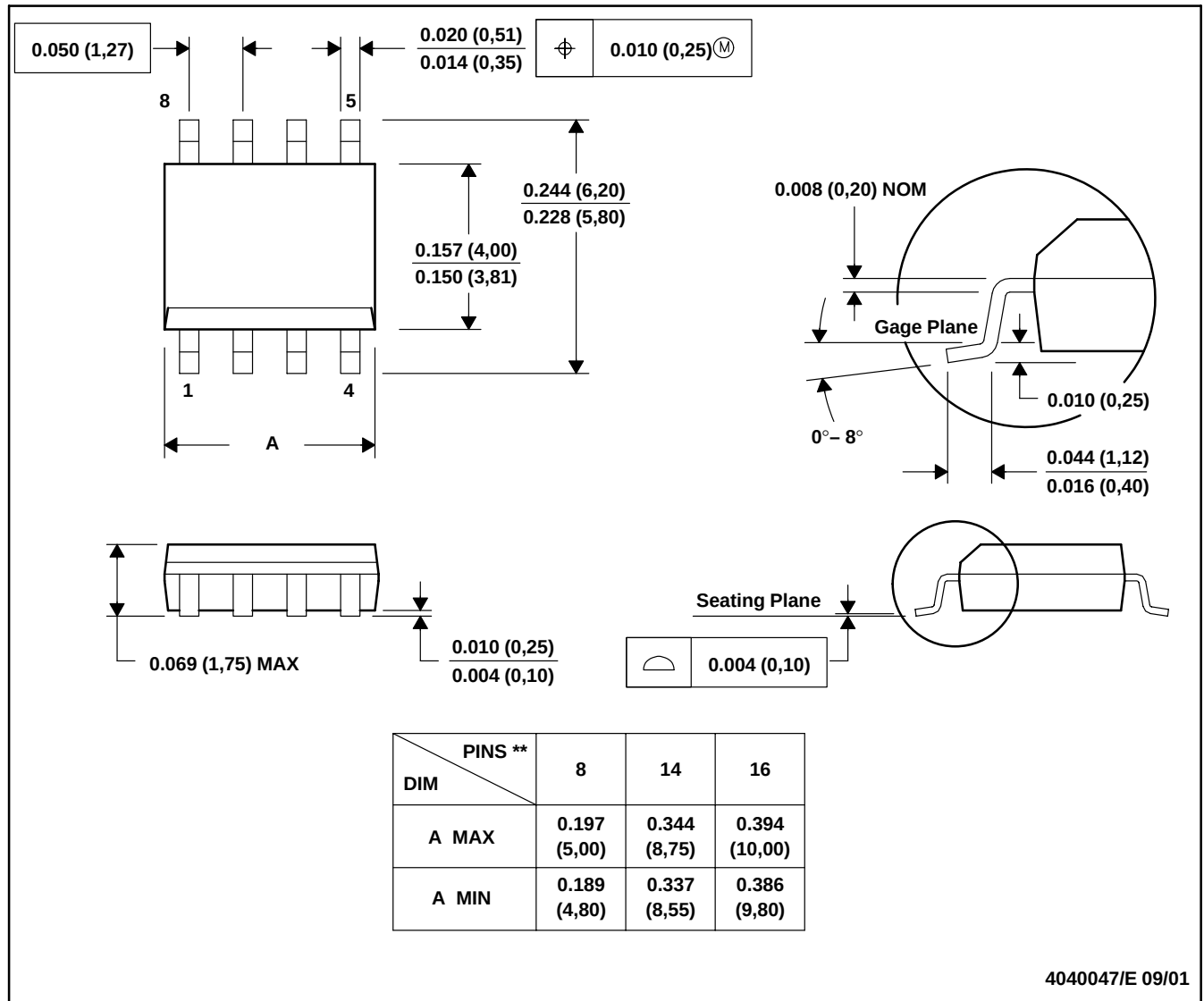


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-178

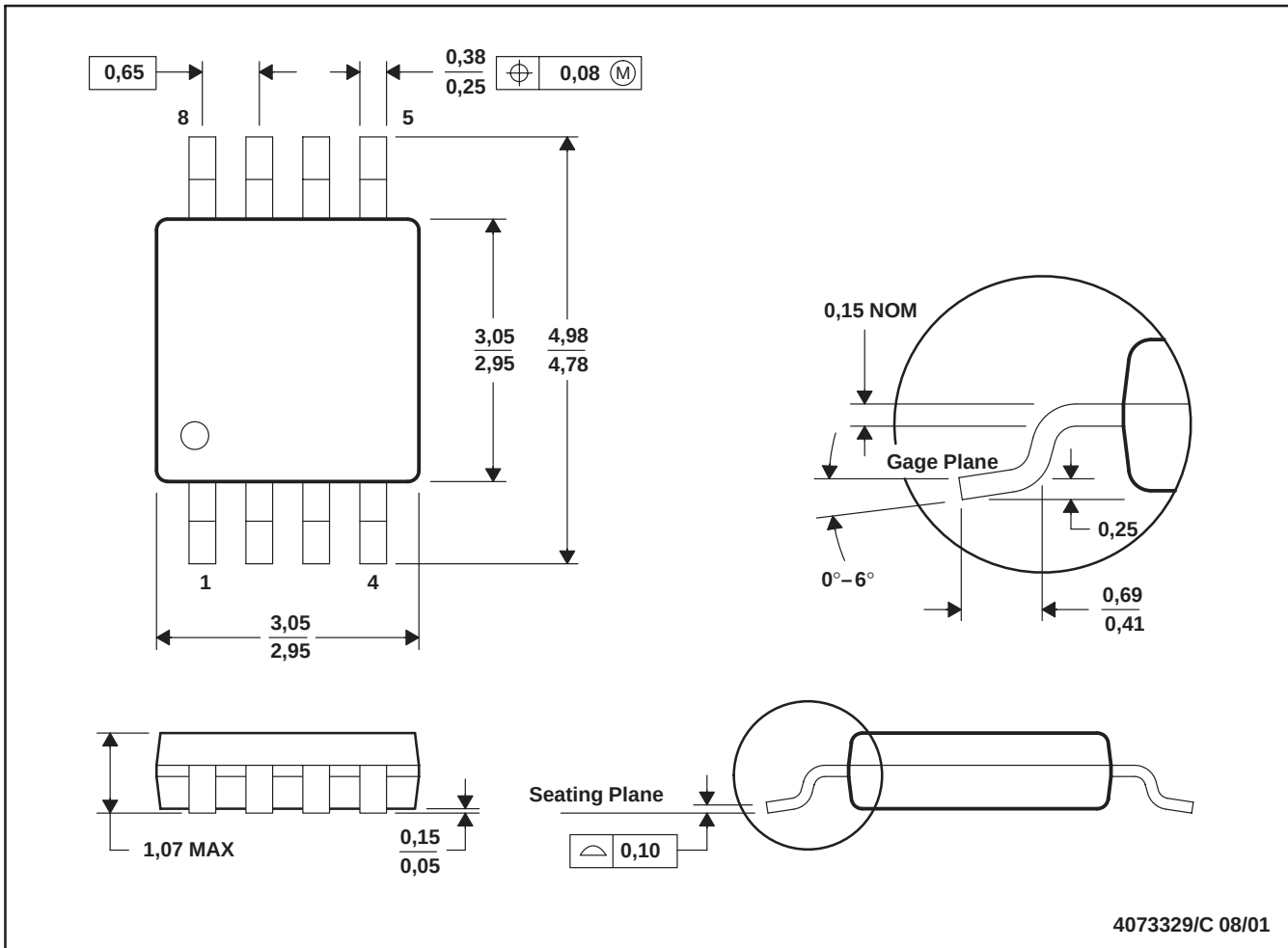
D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-012



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2334AIDGSR	Active	Production	VSSOP (DGS) 10	2500 LARGE T&R	Yes	Call TI Nipdauag	Level-2-260C-1 YEAR	-40 to 125	BHE
OPA2334AIDGSR.Z	Active	Production	VSSOP (DGS) 10	2500 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BHE
OPA2334AIDGST	Active	Production	VSSOP (DGS) 10	250 SMALL T&R	Yes	Call TI Nipdauag	Level-2-260C-1 YEAR	-40 to 125	BHE
OPA2334AIDGST.Z	Active	Production	VSSOP (DGS) 10	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BHE
OPA2335AID	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2335
OPA2335AID.Z	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2335
OPA2335AIDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHF
OPA2335AIDGKR.Z	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHF
OPA2335AIDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAUAG SN	Level-2-260C-1 YEAR	-40 to 125	BHF
OPA2335AIDGKT.Z	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BHF
OPA2335AIDGKTG4	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHF
OPA2335AIDGKTG4.Z	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHF
OPA2335AIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2335
OPA2335AIDR.Z	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2335
OPA2335AIDRG4.Z	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2335
OPA334AIDBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OAOI
OPA334AIDBVR.Z	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OAOI
OPA334AIDBVRG4	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OAOI
OPA334AIDBVT	Active	Production	SOT-23 (DBV) 6	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OAOI
OPA334AIDBVT.Z	Active	Production	SOT-23 (DBV) 6	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OAOI
OPA334AIDBVTG4.Z	Active	Production	SOT-23 (DBV) 6	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OAOI
OPA335AID	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 335
OPA335AID.Z	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 335
OPA335AIDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAPI

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA335AIDBVR.Z	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAPI
OPA335AIDBVRG4.Z	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAPI
OPA335AIDBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAPI
OPA335AIDBVT.Z	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAPI
OPA335AIDBVTG4	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAPI
OPA335AIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 335
OPA335AIDR.Z	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 335
OPA335AIDRG4.Z	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 335

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF OPA2335 :

- Military : [OPA2335M](#)

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications

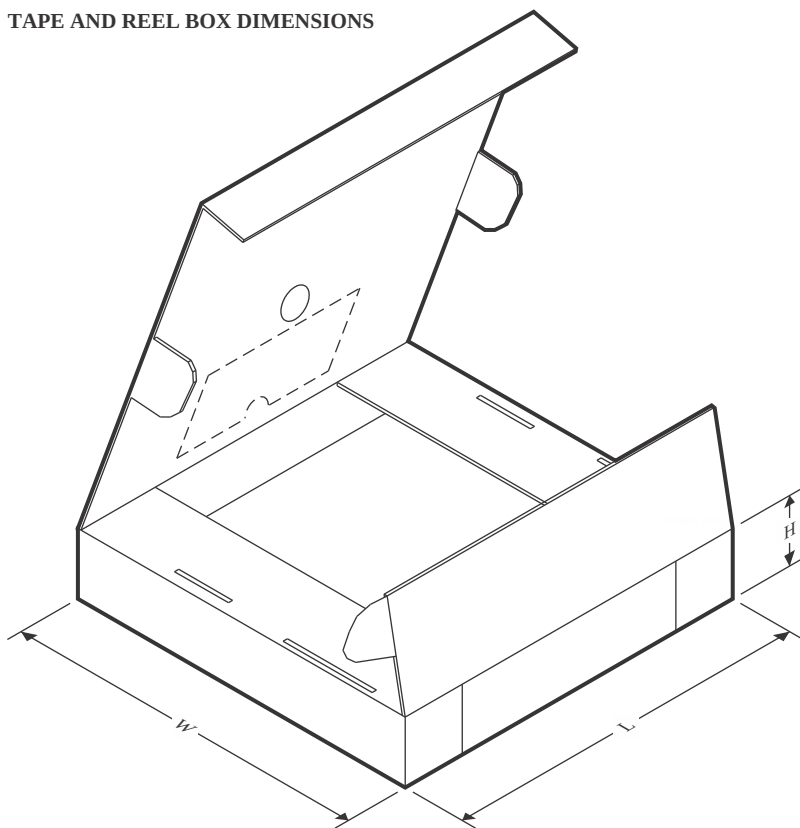
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2335AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2335AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2335AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2335AIDGKTG4	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2335AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA334AIDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA334AIDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA335AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA335AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA335AIDBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA335AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

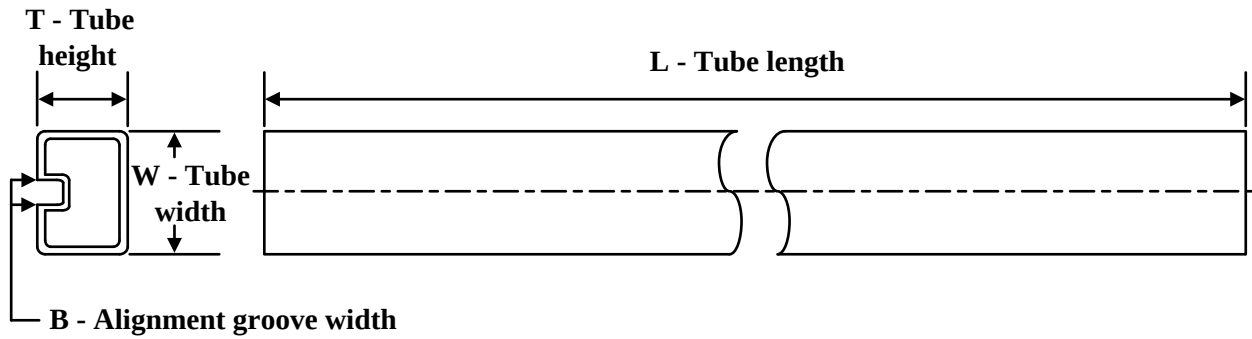
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

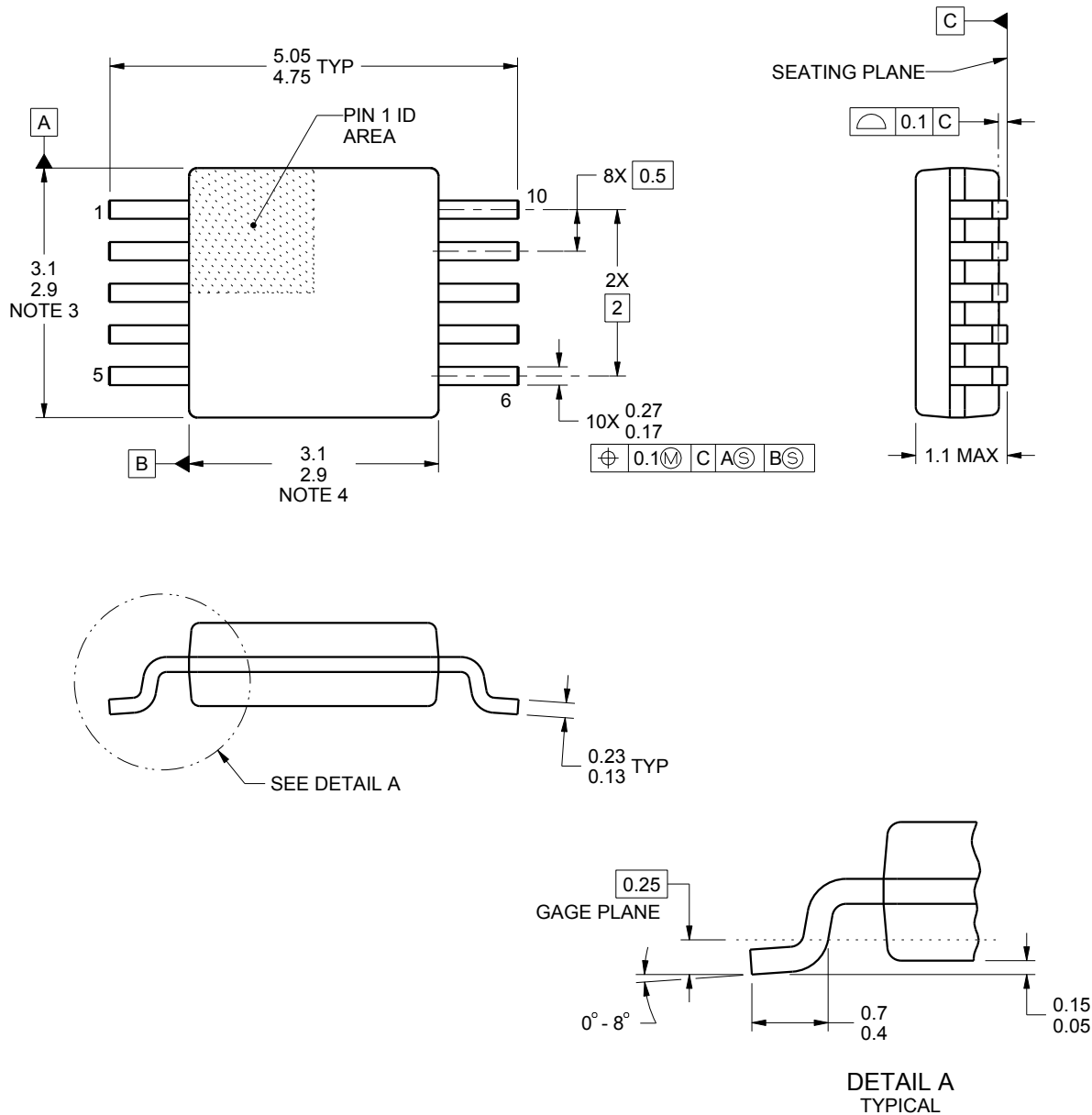
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2335AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2335AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2335AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2335AIDGKTG4	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2335AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA334AIDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
OPA334AIDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
OPA335AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA335AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA335AIDBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
OPA335AIDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA2335AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2335AID.Z	D	SOIC	8	75	506.6	8	3940	4.32
OPA335AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA335AID.Z	D	SOIC	8	75	506.6	8	3940	4.32



4221984/A 05/2015

NOTES:

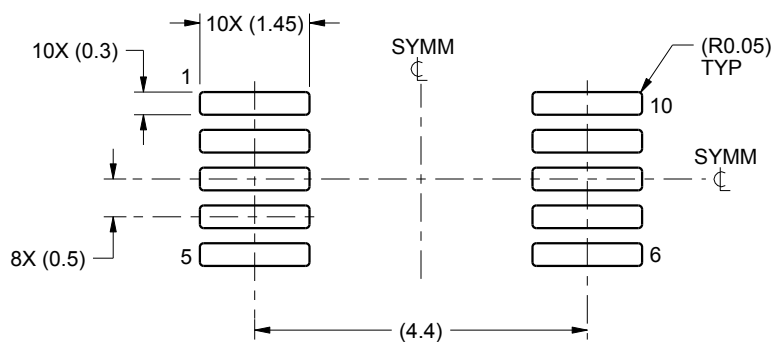
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

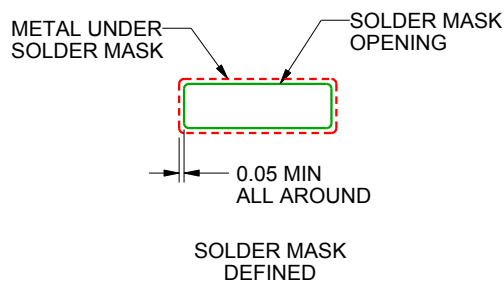
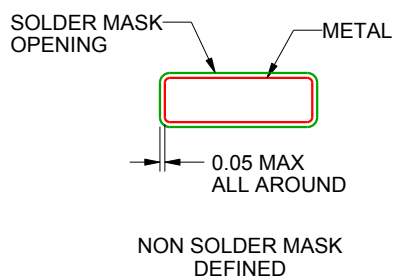
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

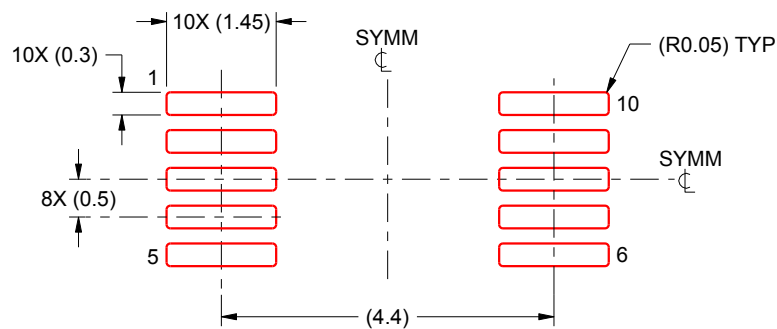
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

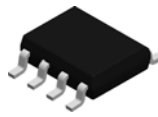


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

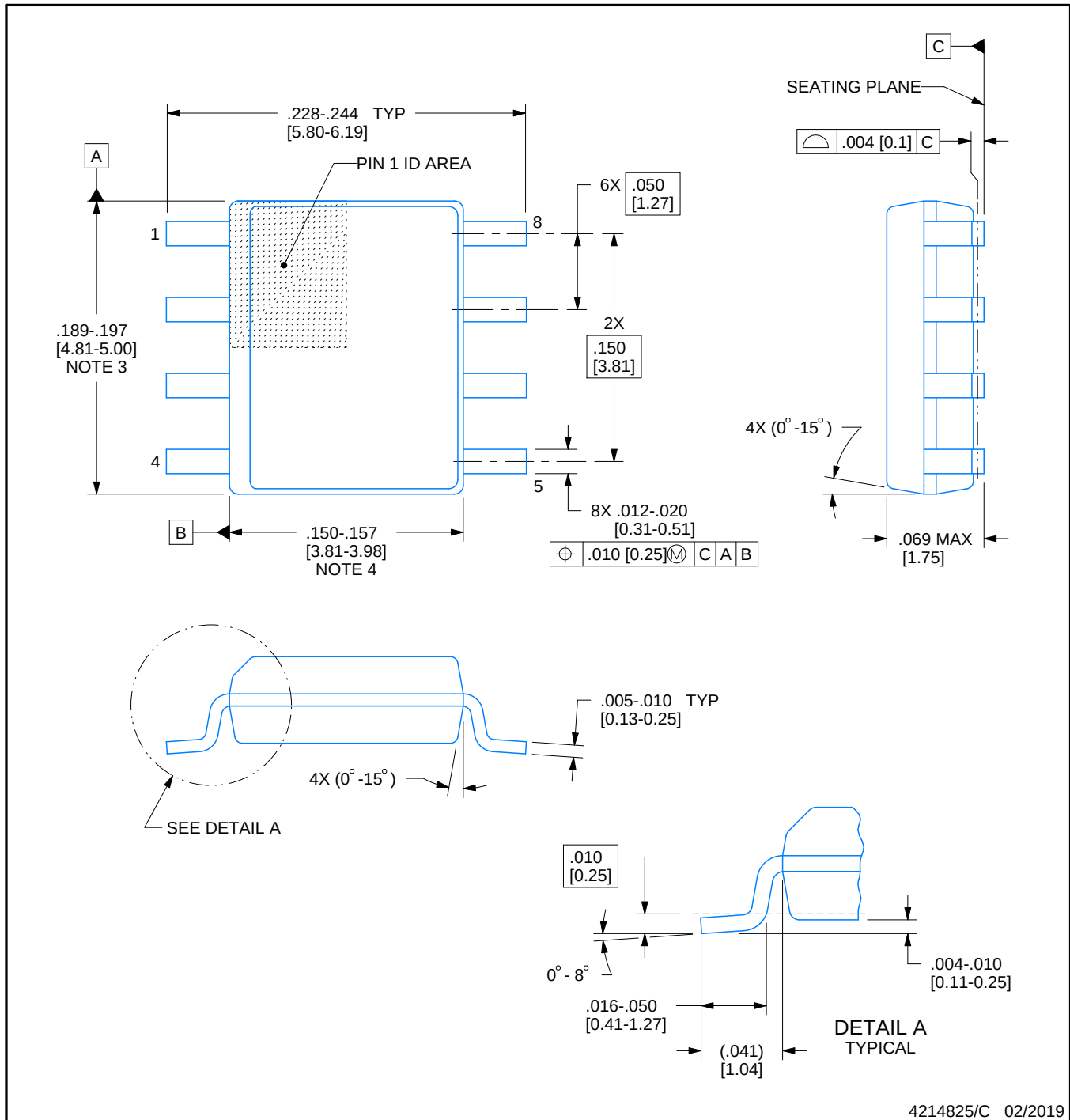


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

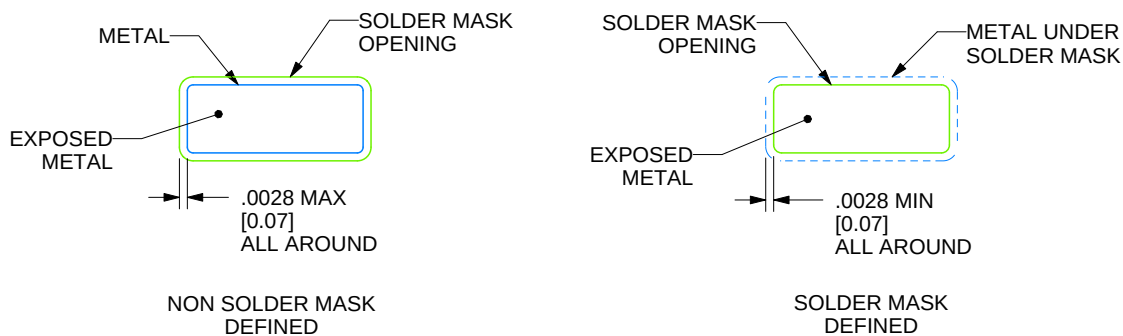
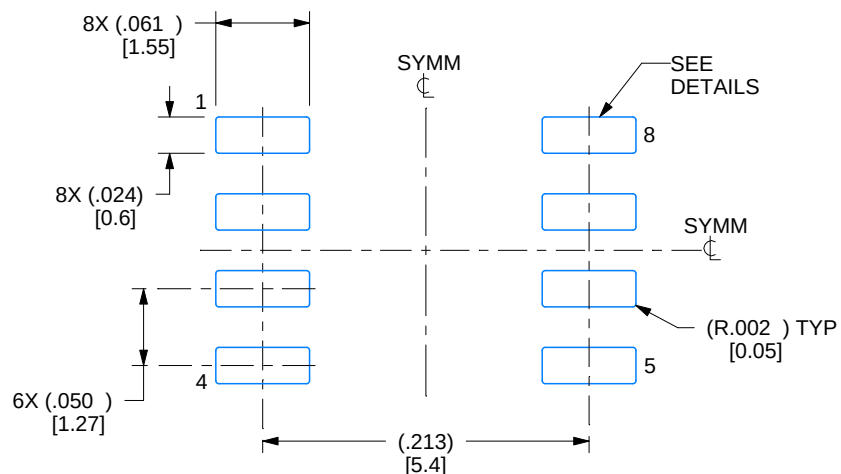
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

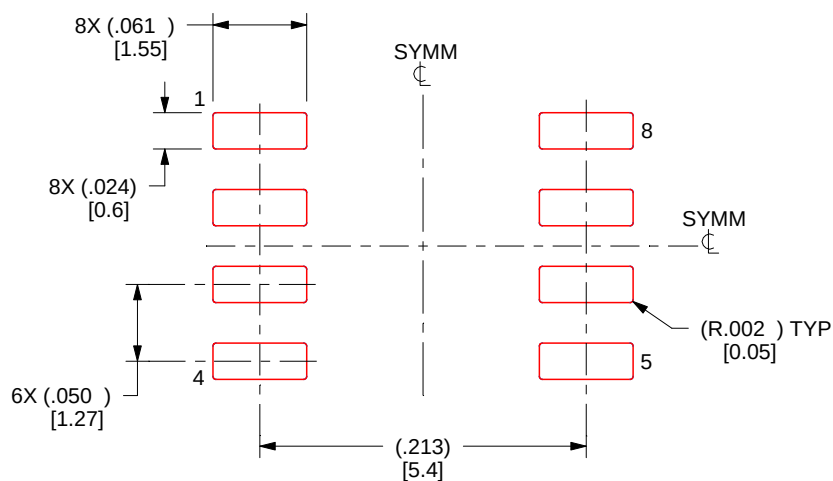
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

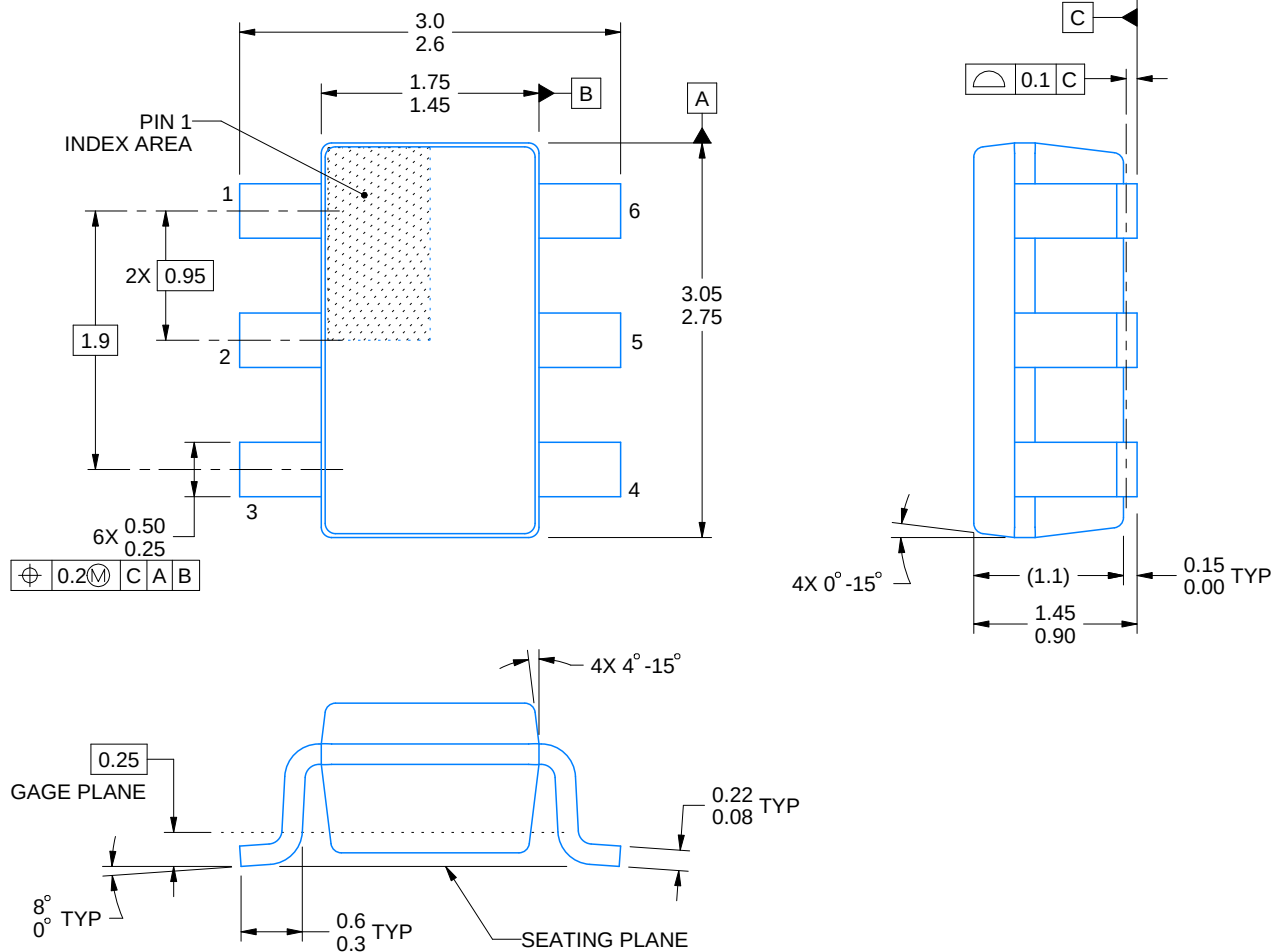
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DBV0006A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

NOTES:

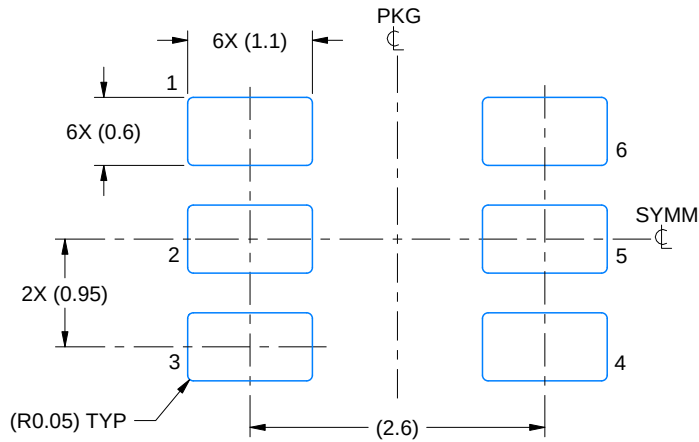
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

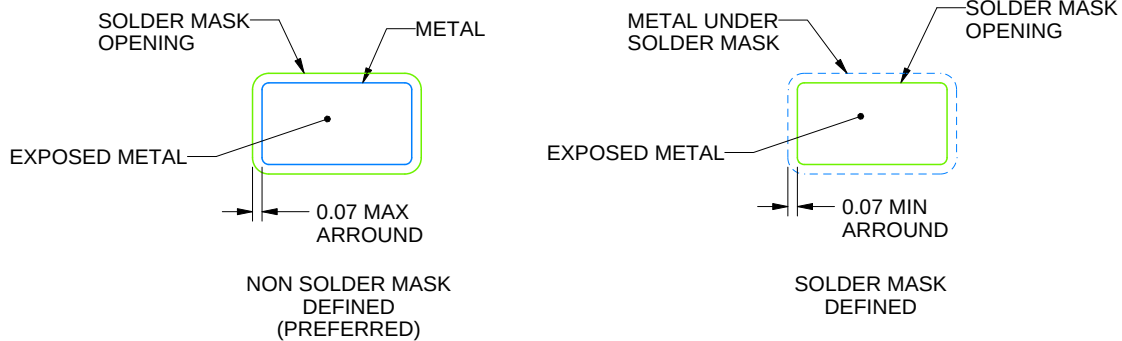
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

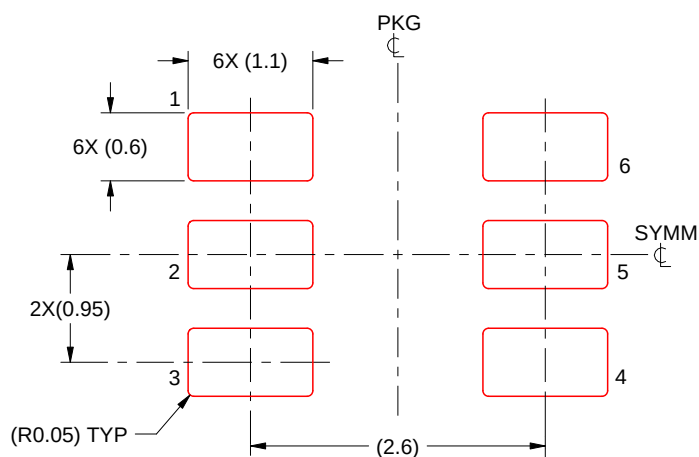
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

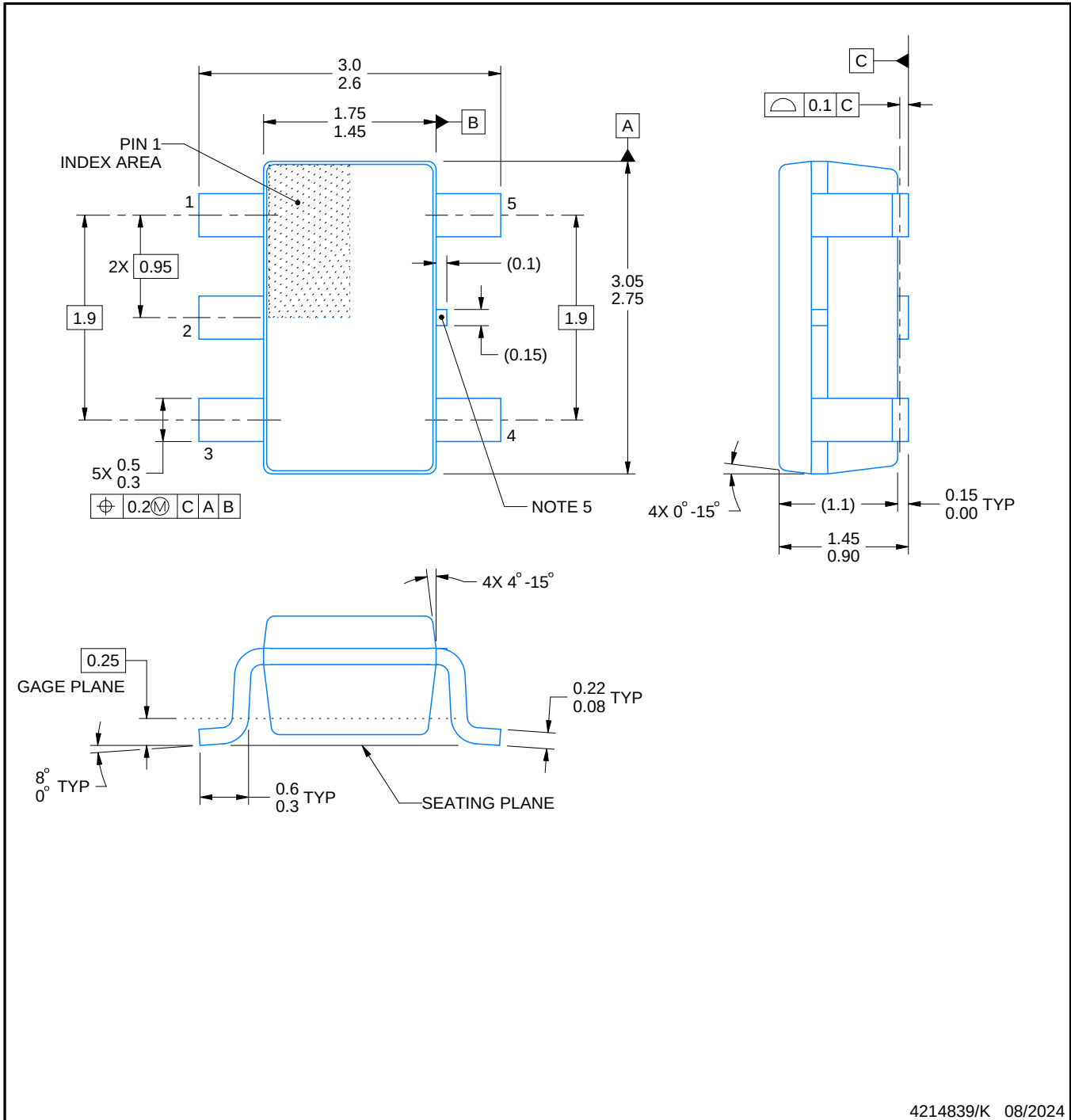


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

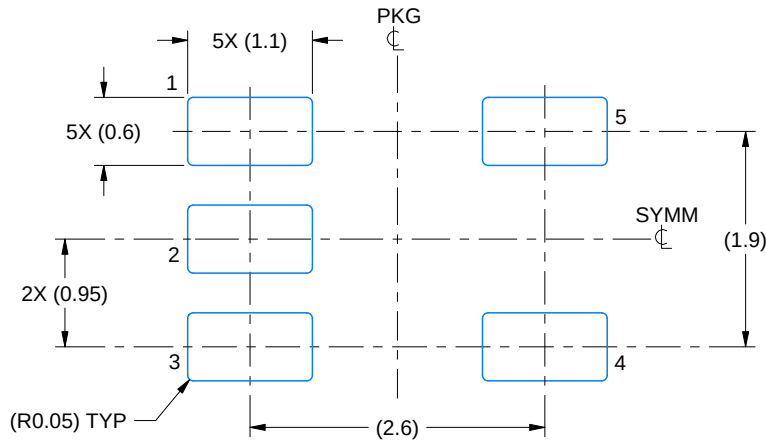
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

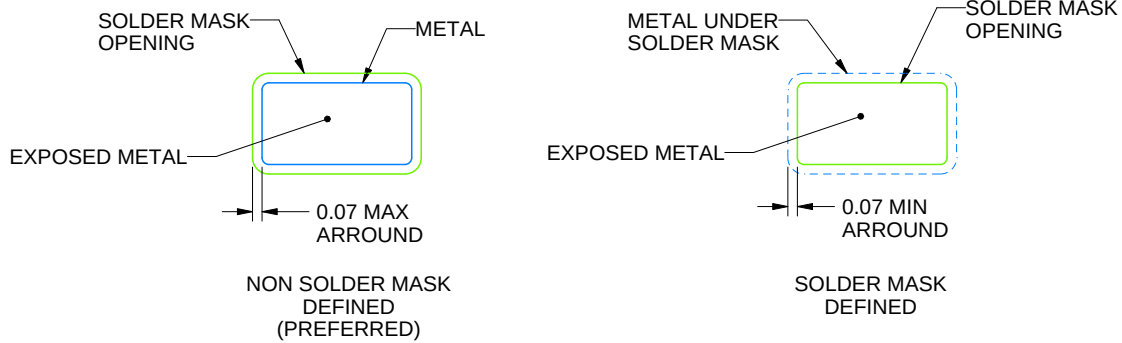
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

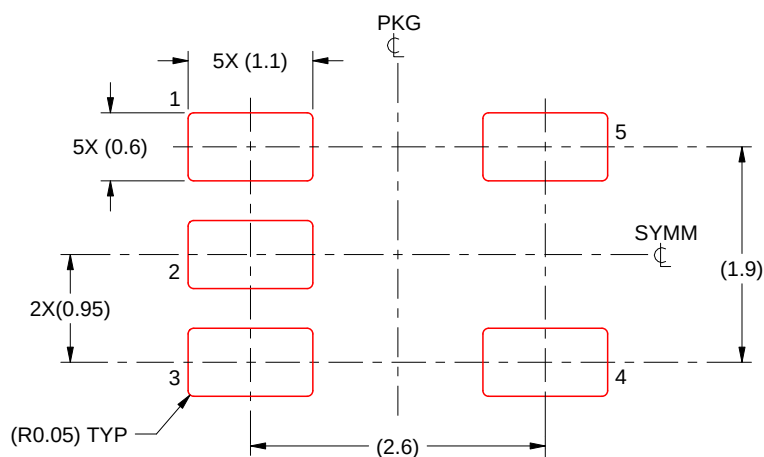
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



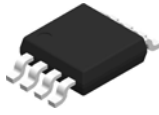
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

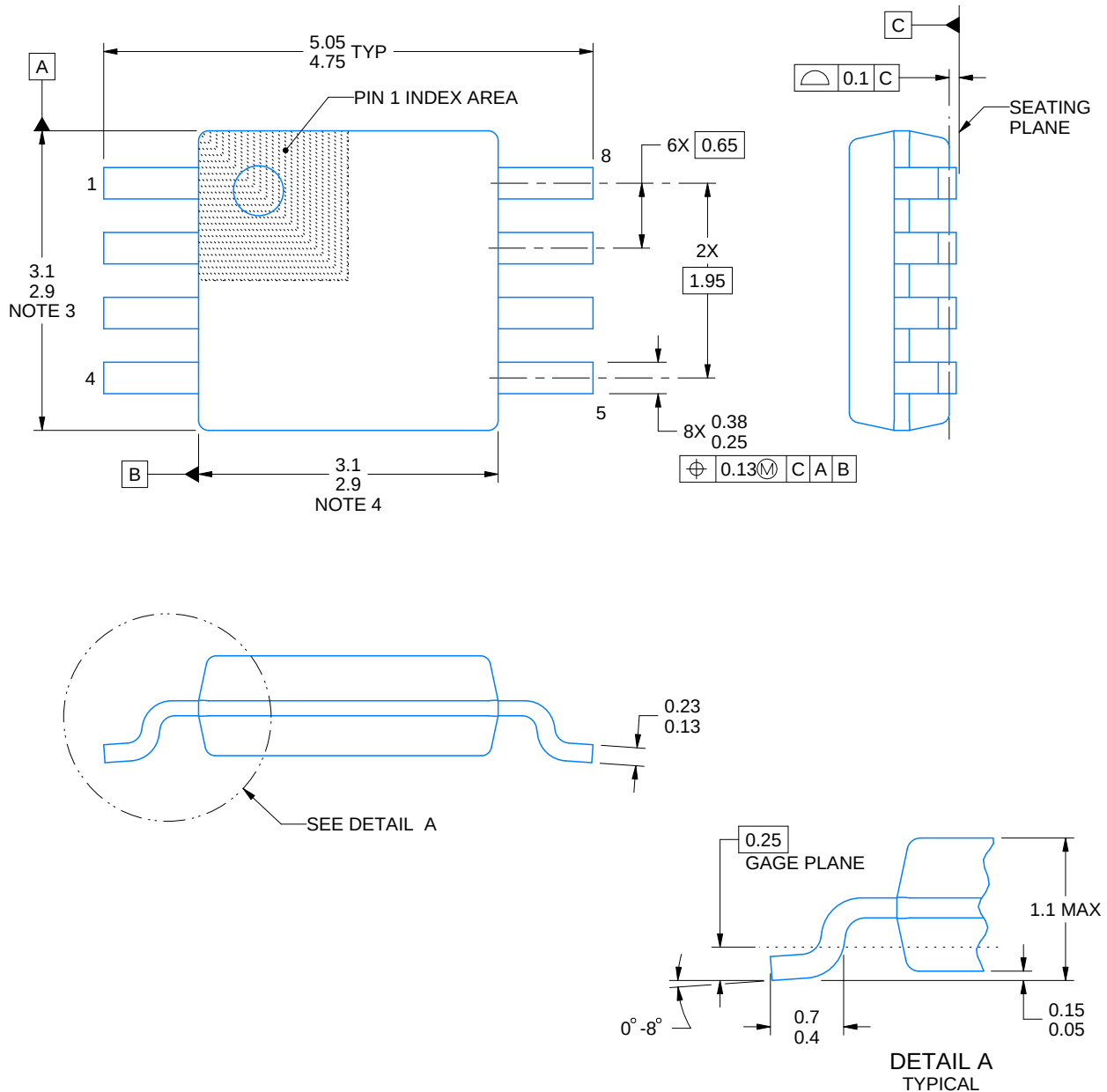
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

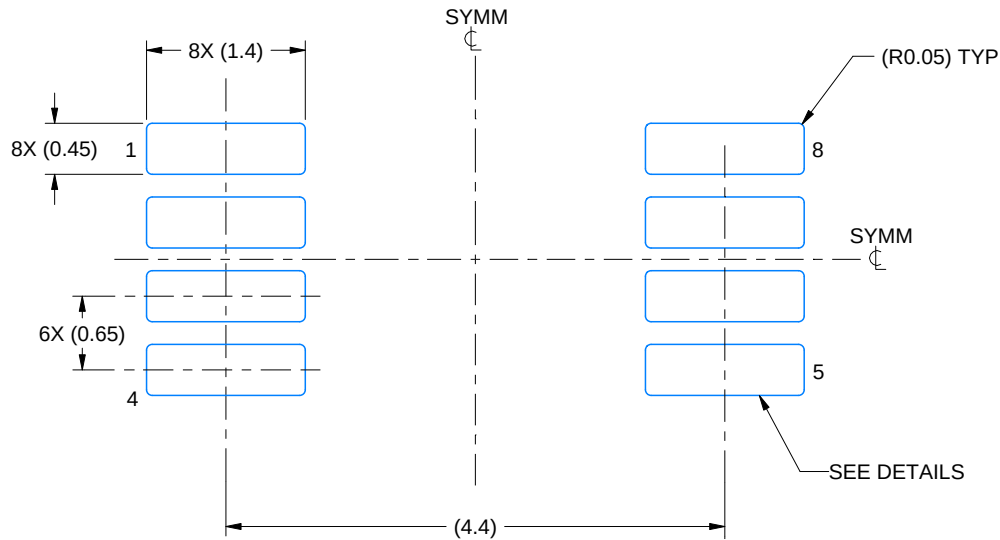
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

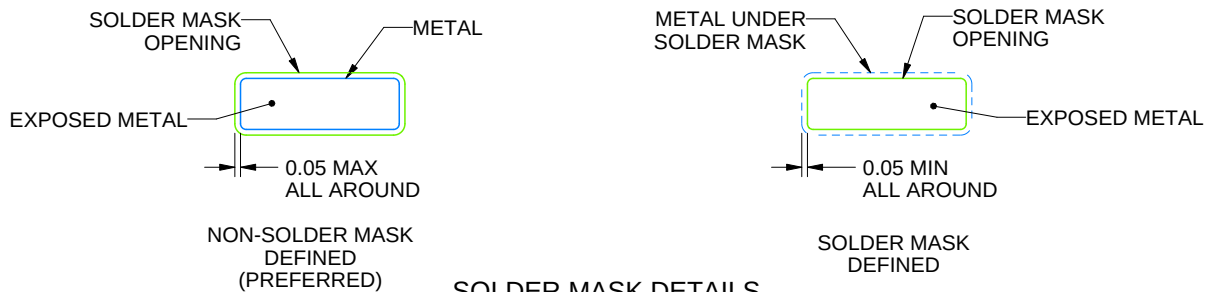
DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

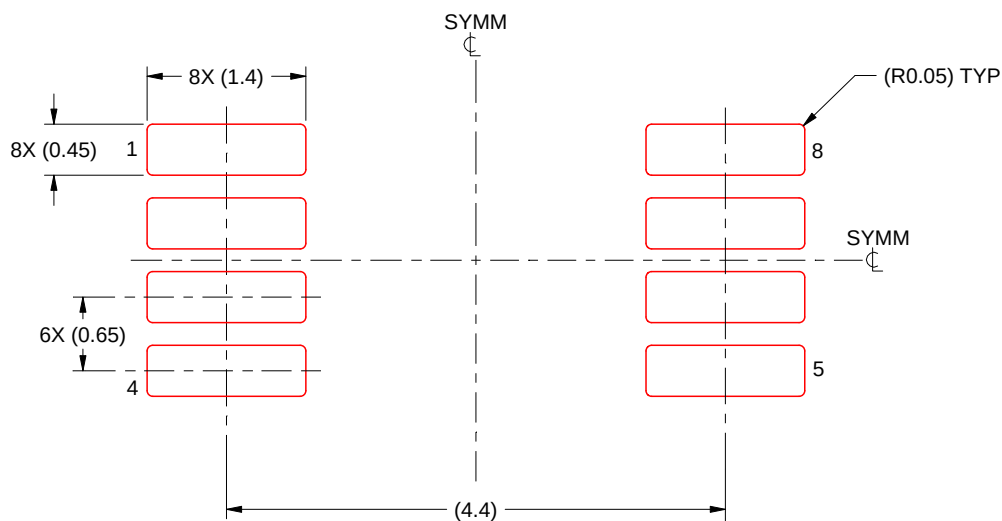
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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